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Explicit characterization of bandgap references

Xin Dai
Iowa State University

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Xin Dai

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Randall L. Geiger (Major Professor)
Degang Chen
Zhengdao Wang

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ABSTRACT

Stable and precision voltage references are an integral part of many analog and mixed-signal integrated circuits. Bandgap references have been widely used for precision on-chip voltage sources in both bipolar and CMOS processes. Conspicuously absent in the literature are explicit relationships between the output voltage and temperature of bandgap references. Temperature characteristics of bipolar junction transistors (BJT's) are developed to explicitly characterize the I-V relationship of BJT's. Based on this characterization, an explicit relationship for the output voltage of a popular bandgap reference structure is developed. Within the context of this explicit relationship, temperature stability properties of references are explored.

Also included in this work is the introduction of a new digital calibration algorithm for pipeline ADCs and an order-dependent layout strategy that inherently cancels high-order gradient effects. The digital calibration algorithm does not require perturbation of the signal path through the pipeline and requires only code density test data generated from applying a simple non-critical test signal at the input. This calibration algorithm can be used to calibrate a multitude of ADC architectures. As a practical example, this method is used to calibrate a sub-radix pipeline ADC with minimal digital circuit overhead. By incorporating this calibration algorithm as part of the design process, the design requirements of the analog part of an ADC can be relaxed. The n^{th} order central-symmetrical layout method provides cancellation of all spatial gradients up to n^{th} order by using 2^n unit cells in each element for pair-wise element matching. This method is useful for the layout of matching critical devices in high-precision circuits.

CHAPTER 1 INTRODUCTION

Since the birth of the first transistor in Bell Laboratories in 1947, the semiconductor industry has experienced explosive growth which has caused dramatic changes to peoples' daily life. Nowadays, integrated circuits (IC's) are present in many places from cell phones and PCs to large computer controlled systems such as aircraft and satellites. Advances in both design and fabrication technologies are doubling the integration density every 24 months as Moore predicted forty years ago. As a result, more functions are being integrated into a smaller chip area and improvements in speed and power dissipation are continuously being made. Paralleling the rapid development of the semiconductor industry, analog and mixed signal systems (AMS) are gaining a lot of attention. The unrelenting pursuit for improvements in system performance is resulting in more stringent linearity, noise, and power consumption requirements. However, the design of these AMS systems is still pretty much manual because the large amounts of innovation, creativeness, and performance tradeoffs required in these designs is difficult to capture in a synthesis-based computer-aided design (CAD) framework. As feature sizes continue to shrink, both device characterization and process control become more difficult, making the design job even more challenging.

My work at Iowa State University has been focused on several challenges related to the design of high performance circuits. The major part of this thesis will be focused on explicit characterization of bandgap references. A stable and precision voltage reference or current reference is essential in many analog and mixed-signal integrated circuits and systems. The increasing performance requirements of these circuits driven by a host of lucrative applications have raised the accuracy and temperature stability requirement for the

references. Bandgap references have been and will continue to be widely used for precision on-chip voltage sources. A study of bandgap reference designs reported in the literature along with the comparative strengths and weaknesses of the varying approaches is necessary for the practical design of high performance references. In all of the bandgap references considered in this study which likely included all of the widely used references and several less-popular structures, we observed the conspicuous absence of an explicit relationship between the output voltage and temperature. The conventional approach to designing bandgap references which is based upon an expression for the reference output voltage that involves circuit variables dependent on the reference circuit itself does not give much insight into the merits of a design and does not provide a method for making fair comparisons between different bandgap architectures. In this work, the temperature characteristics of BJT's and correspondingly the temperature characteristics of bandgap references are developed in a way that provides an explicitly characterization for the output voltage of the bandgap references. Within the context of this explicit relationship, temperature stability properties of references are explored. The explicit relationship provides improved insight into performance potential and limitations of bandgap architectures and is useful for the design of high-performance bandgap references.

Another part of my work includes the development of a digital calibration algorithm for calibrating pipeline ADCs. The randomness in fabrication processes causes errors in matching-critical circuits. This effect becomes more problematic as feature sizes go down and performance requirement goes up. As a result, design techniques for making robust designs insensitive to these errors are highly desired. One of the most promising ways of doing this is to make the analog part as simple as possible and take advantage of digital

calibration to calibrate the error out. In many data converter circuits, the analog portion consumes more area than the digital part, and with most existing approaches, the analog area increases geometrically with linear increases in specifications. Considering that silicon area in advanced fabrication process is getting more and more expensive while yield is invariably inversely proportional to chip area, allocating more area to the analog part of an integrated circuit is not a favorable solution. In contrast, making the analog part simple, which is equivalent to making the chip size smaller, is a much more appealing approach. In addition to the savings in area and cost, making the analog part simple eases the design since analog designs are usually not automated while many of the digital parts of a circuit can be synthesized with CAD tools. Simpler analog designs often come with smaller devices and as a result, reduced parasitics. This is very attractive in applications with high speed requirements and stringent frequency domain specifications. In the literature, there have been repeated attempts at using calibration to improve the performance of high-resolution data converters, including some impressive work from Iowa State. Unfortunately, experimental results obtained with most of these structures do not provide performance at a level that is competitive with what is attainable with good non-calibrated designs coming from industry today and thus industrial adoption of these calibration methods is limited. This is, in part, due to the complexity of some of the calibration algorithms, due to the dependence of some methods on model accuracy, and due to the interruptions of the signal path internal to the data converter required for implementation of the calibration algorithms. The digital calibration algorithm I propose is based upon the output of a standard histogram test generated from applying imprecise test signals directly to the input of the ADC without any interruption of the flow of signals internal to the pipeline. With this approach, a pipeline

ADC can be calibrated with only a small implementation overhead. By doing this, the design requirements for the analog portion of the ADC can be relaxed while achieving exacting performance with the calibration.

Also included in this thesis is a new layout technique for improved matching accuracy. After the schematic design and functional verification is completed, a layout of the circuit must be generated. In matching-critical applications, layout is very important and plays a key role in the performance or yield that is ultimately obtained. Poor layout techniques can totally ruin a very good circuit design and even those that are very experienced at matching-critical layout are limited by the lack of proven methods that will maintain good matching in the presence of higher-order gradients of process parameters inherent in essentially all fabrication processes. We have recently introduced a new layout method [1] that offers potential for yield enhancement in matching-critical applications with some promising results. The layout method I am introducing has a very simple topology that can be used to cancel high-order gradients in parameters of circuit elements such as those in the models of MOS transistors or higher-order gradients in resistors or capacitors thus providing better matching accuracy than is attainable with the widely-used common-centroid layout techniques that only provide cancellation of mismatch associated with linear gradients. .

The organization of the thesis is as follows. A study and explicit characterization of bandgap references is presented in Chapter 2. This is an extension of work presented at the 2006 IEEE International Symposium on Circuits and Systems (ISCAS 2006) [2]. Chapter 3 is comprised of a description of the digital calibration algorithm for calibrating pipeline ADCs. This is based on a paper presented at ISCAS 2005 [3]. A layout strategy for canceling

gradient effects, which is based on another paper presented at ISCAS 2005 [4] and some subsequent results are discussed in Chapter 4. Chapter 5 constitutes conclusions.

CHAPTER 2 EXPLICIT CHARACTERIZATION OF BANDGAP REFERENCES

2.1 Introduction

A stable and precision voltage reference is an essential part in many analog and mixed-signal integrated circuits and systems such as phase-locked loops (PLLs), memories and data converters. Since its introduction by Widlar [5] in the 1970's, the basic bandgap reference and its different variations [6-9] have been widely used in the implementation of on-chip precision voltage reference sources in bipolar and CMOS processes. Over the years since the work of Widlar, considerable effort has been made on improving the performance of basic bandgap circuits to meet the ever-increasing temperature stability requirements or specific needs from different applications. Different techniques such as laser trimming [6,7], curvature compensation [10-12], op amp offset cancellation [11], etc, have been employed individually or jointly to minimize the temperature drift of the reference voltage in continuous-time or discrete-time systems. In addition, new architectures [9,13] have been developed which provide for extensions to low voltage or current mode applications.

In spite of the continuous technology innovation and the ensuing performance improvements, not much attention has been focused towards the theoretical analysis and characterization of bandgap references and hence little progress has been made in the field. The formulations that almost every author of the works mentioned above used when introducing their circuits were almost the same as what came with the proposing of the basic bandgap reference concept more than 30 years ago. The expression of the reference voltage

usually involves a BJT's base-emitter voltage, which is a function of the current flowing in the device, and neither a process parameter nor a design parameter. These formulations involving convenient parameters did a good job in demonstrating the concept but failed to provide a closed form explicitly expression for the reference voltage, making it difficult to determine the performance potential and limitations of different structures and making it difficulty to fairly compare the relative merits of the different architectures that have appeared in the literature. Accurate modeling is essential for understanding and characterizing the bandgap circuit, especially as the temperature stability requirements increase.

This work addresses the issue of analytical characterization of bandgap references. An explicit model of the circuit and formulations only involving process and model parameters is derived after an investigation of the I/V characteristics of bandgap references. The temperature stability of bandgap reference is then analyzed based on this model.

The rest of the chapter is organized as follows. The modeling of temperature dependence of the BJT is discussed in Section 2.2. A review of the bandgap reference concept is presented in Section 2.3. Analytical modeling and explicit characterization of a bandgap circuit along with a practical example are given in Section 2.4. A conclusion of this work comprises Section 2.5.

2.2 Temperature Dependent BJT Model

The BJT (or pn junction) is widely used in bandgap reference design because of the special temperature characteristics of the pn junction. Although nowadays most of the larger analog and mixed-signal circuits are fabricated in CMOS processes and use only MOS

transistors, the bandgap reference is usually an exception where either a parasitic BJT or a pn junction is used for the temperature-sensitive part of the bandgap reference. There has been some research on CMOS only references that do not use a pn junction , but the BJT (or pn junction) is still overwhelming the device of choice in bandgap design because of what most believe is better performance and lower design complexity. A study of the BJT's temperature characterization is fundamental to BJT-based bandgap reference design.

The collector current and the base-emitter voltage of a BJT has an exponential relationship given by

$$I_C = I_S e^{V_{BE}/V_T}, \tag{2.1}$$

where I_S is the saturation current, $V_T = kT/q$, k is Boltzman's constant, T is the temperature in K and q is the charge of an electron. The parameter I_S is a process and design parameter and can be expressed as

$$I_S = J_S A, \tag{2.2}$$

where J_S is a geometry-independent process parameter and A is the area factor of the device, determined by the sizing of the device. Trivially, it follows from (2.1) and (2.2) that

$$I_C = J_S A e^{V_{BE}/V_T}. \tag{2.3}$$

The temperature dependence of the relationship between V_{BE} and I_C is significant but beyond the component due to V_T. This is not apparent from (2.1) since a significant portion of the temperature dependence is embedded in the parameter I_S.

If the temperature dependence of I_S is included, it can be shown that the relationship between collector current density and the base-emitter voltage at a temperature T is related to that at a temperature T_0 by the expression [5]

$$V_{BE}(T) = V_{G0}\left(1-\frac{T}{T_0}\right)+V_{BE}(T_0)\frac{T}{T_0}+\frac{mkT}{q}\ln\left(\frac{T_0}{T}\right)+\frac{kT}{q}\ln\left(\frac{J_C(T)}{J_C(T_0)}\right), \qquad (2.4)$$

where V_{G0} is the bandgap voltage, J_C is the collector current density and m is a temperature independent constant.

Equation (2.4) is useful for relating the operating point at a temperature T to that at a temperature T_0. The terms $J_C(T_0)$ and $V_{BE}(T_0)$ in (2.4) are convenient to use but are related to each other and are both functions of the current flowing in the device. As such, neither is a process parameter nor a design parameter. Almost all authors simply gloss over this fact and do not address what information is really carried in these terms or where they come from. Regardless, the functional form of (2.4) is widely and almost exclusively used when bandgap references are discussed [5-7]. It is important to emphasize that (2.4) should not be viewed as an equation that models the BJT (or diode) because the parameters $J_C(T_0)$ and $V_{BE}(T_0)$ are not model or port variable parameters.

Equation (2.4) does not look like the standard diode equation but the relationship to the standard diode equation becomes apparent by rewriting (2.4) as

$$I_C(T) = J_C(T_0)Ae^{\frac{V_{BE}(T_0)}{V_{T0}}}\left(\frac{T}{T_0}\right)^m e^{\frac{V_{G0}}{V_T}\left(\frac{T}{T_0}-1\right)\frac{V_{BE}(T)}{V_T}}, \qquad (2.5)$$

where $I_C(T)$ is the collector (or diode) current, $V_{T0}=kT_0/q$, and A is the emitter area factor. The standard parameter I_S of (2.1) that appears in the diode equation is thus

$$I_S(T) = J_C(T_0) A e^{\frac{V_{BE}(T_0)}{V_{T_0}}} \left(\frac{T}{T_0}\right)^m e^{\frac{V_{G0}}{V_T}\left(\frac{T}{T_0}-1\right)}. \tag{2.6}$$

The temperature dependence on I_S is explicitly shown in this equation. Actually, SPICE uses a slightly different partitioning of (2.5) as shown in (2.7)

$$I_C(T) = \left\{\left[J_C(T_0) A e^{\frac{V_{BE}(T_0)}{V_{T_0}}}\right]\left(\frac{T}{T_0}\right)^m e^{\frac{V_{G0}}{V_T}\left(\frac{T}{T_0}-1\right)}\right\} e^{\frac{V_{BE}(T)}{V_T}}. \tag{2.7}$$

If the term in brackets in (2.7) is defined to be the parameter I_{SX}, that is

$$I_{SX}(T_0) = \left[J_C(T_0) A e^{\frac{V_{BE}(T_0)}{V_{T_0}}}\right], \tag{2.8}$$

then it follows from (2.7) and (2.8) that the current can be expressed as

$$I_C(T) = \left\{I_{SX}(T_0)\left(\frac{T}{T_0}\right)^m e^{\frac{V_{G0}}{V_T}\left(\frac{T}{T_0}-1\right)}\right\} e^{\frac{V_{BE}(T)}{V_T}}. \tag{2.9}$$

The parameter $I_{SX}(T_0)$ is a model parameter that is only dependent upon the process and the geometry of the device and (2.9) is a model equation that characterizes the device. The choice of the temperature at which the parameter I_{SX} is defined is arbitrary but must be the same as the temperature T_0 used in (2.9). Note that neither of the parameters $J_C(T_0)$ and $V_{BE}(T_0)$ appear in (2.9) however a relationship between these parameters can be seen by referring to (2.8).

Since the choice of the temperature used is arbitrary, the model of (2.9) is not dependent upon T_0. To show this, first, rewrite (2.9) as

$$I_C(T) = \left\{ I_{SX}(T_0) T_0^{-m} e^{\frac{qV_{G0}}{kT_0}} \right\} \left[T^m e^{\frac{V_{BE}(T) - V_{G0}}{V_T}} \right]. \tag{2.10}$$

In (2.10), notice that all the T_0 dependent terms are included in the braces and the term in brackets is not dependent upon T_0. Since $I_C(T)$ is not dependent on T_0, the term in braces must be independent of T_0, even though the expression does not look like a T_0 independent term. If we define the term in braces to be $\tilde{I}_{SX}$, that is

$$\tilde{I}_{SX} = I_{SX}(T_0) T_0^{-m} e^{\frac{qV_{G0}}{kT_0}}. \tag{2.11}$$

Then, substituting (2.11) back to (2.10) gives

$$I_C(T) = \left(\tilde{I}_{SX} \left[T^m e^{\frac{-V_{G0}}{V_T}} \right] e^{\frac{V_{BE}(T)}{Vt}} \right). \tag{2.12}$$

It may be useful to explicitly show the dependence of the emitter area on the collector current. To show this explicitly, define the term $\tilde{J}_{SX}$ by the expression

$$\tilde{J}_{SX} = \frac{\tilde{I}_{SX}}{A}, \tag{2.13}$$

where A is the emitter area. Then (2.12) can be expressed as

$$I_C(T) = \left(\tilde{J}_{SX} A \left[T^m e^{\frac{-V_{G0}}{V_T}} \right] \right) e^{\frac{V_{BE}(T)}{V_T}}. \tag{2.14}$$

$\tilde{J}_{SX}$ is a process parameter and since the model is independent of T_0, it must be concluded that is independent of T_0. Comparing (2.3) and (2.14), it is apparent that

$$J_S = \tilde{J}_{SX}\left[T^m e^{\frac{-V_{G0}}{V_T}}\right]. \tag{2.15}$$

It is often more convenient to work with a model equation that has an explicit expression for V_{BE}. Exponentiating (2.3), an equivalent model equation is

$$V_{BE} = V_T \ln(I_C) - V_T \ln(J_S A). \tag{2.16}$$

Substituting (2.15) into (2.16) gives

$$V_{BE} = V_T \ln(I_C) + \left(V_{G0} - V_T\left(\ln\left(\tilde{J}_{SX} A\right) + m\ln(T)\right)\right). \tag{2.17}$$

The second term on the right hand side of (2.17) contains no port variables and, as such, when analyzing circuits, it appears as a constant. It is more convenient to represent this constant by a parameter $\tilde{\theta}$. With this notation, V_{BE} can be expressed as

$$V_{BE} = V_T \ln(I_C) + \tilde{\theta}, \tag{2.18}$$

where

$$\tilde{\theta} = V_{G0} - V_T\left(\ln\left(\tilde{J}_{SX} A\right) + m\ln(T)\right). \tag{2.19}$$

The emitter current and the base current will be assumed to be related by the expressions

$$I_C = \alpha I_E \tag{2.20}$$

and

$$I_C = \beta I_B, \tag{2.21}$$

where

$$\beta = \frac{\alpha}{1-\alpha}. \tag{2.22}$$

2.3 Review of Bandgap References

Voltage references are circuits that have an output signal that has units volts that are ideally fixed at some predictable value over the temperature range of interest. Since in reality the voltage on any node in any circuit has some supply voltage and temperature dependence, the variation of the reference voltage due to these environment changes is the most important specification for assessing the performance of a reference.

One of the easiest ways to build a voltage reference is to use a voltage divider to generate a voltage proportional to the power supply. However, since the reference voltage is just a fraction of the power supply, the reference suffers from a poor power supply rejection ratio (PSRR), which means the reference voltage is sensitive to changes in the supply voltage. Other ways of generating a reference voltage includes making use of the threshold voltage of a MOS transistor, or the voltage across a pn junction, or the breakdown voltage of a zener diode. The threshold voltage of a MOS transistor and the voltage across a pn junction usually are quite temperature dependent. The zener breakdown voltage of a diode may exhibit reduced temperature dependence but a good zener diode may not be available in many CMOS processes.

A more temperature stable voltage reference can be built by combining two voltages with different temperature characteristics. The main idea is to generate two intermediate voltages, one with a positive temperature coefficient and one with a negative temperature coefficient and then make the reference output a weighted addition of these two signals

where the weight is chosen so that the sum has a zero temperature coefficient at the desired temperature. The structure of such a reference is shown in Figure 2.1.

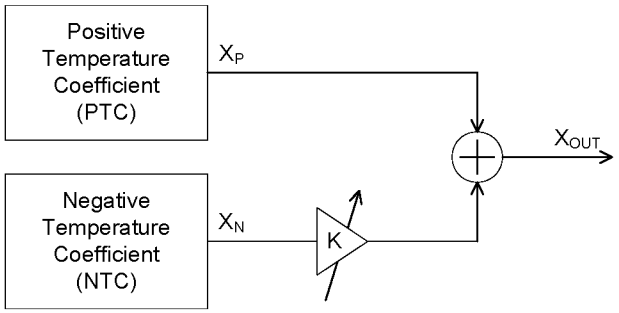

Figure 2.1 Basic structure of temperature stable reference circuits

With this structure, the Positive Temperature Coefficient circuit has an output X_P that satisfies the relationship

$$\frac{\partial X_P(T)}{\partial T} = \psi_P > 0, \tag{2.22}$$

and the Negative Temperature Coefficient circuit has an output X_N that satisfies the relationship

$$\frac{\partial X_N(T)}{\partial T} = \psi_N < 0. \tag{2.23}$$

The output is given by

$$X_{OUT} = X_N + KX_P. \tag{2.24}$$

It thus follows from (2.24) that

$$\frac{\partial X_{OUT}}{\partial T} = \frac{\partial X_N}{\partial T} + K\frac{\partial X_P}{\partial T}. \tag{2.25}$$

The output will have a zero temperature coefficient at the output at a temperature T_{INF} if K in (2.25) is adjusted so that

$$\left.\frac{\partial X_{OUT}}{\partial T}\right|_{T=T_{INF}} = \left.\frac{\partial X_N}{\partial T}\right|_{T=T_{INF}} + K\left.\frac{\partial X_P}{\partial T}\right|_{T=T_{INF}} = 0. \tag{2.26}$$

Bandgap reference is widely used for on-chip reference voltage generation because a well-designed bandgap reference can have very low temperature dependence. A bandgap reference uses V_{BE} of a BJT and the V_{BE} difference between two BJT's as the NTC and PTC part in Figure 2.1 respectively and thus the combination of the two voltages can be quite stable if K is chosen properly.

It follows from (2.17) that the base-emitter voltage of transistor can be expressed as

$$V_{BE} = V_{G0} + \left(V_T\left(\ln\left(I_C\right) - \ln\left(\tilde{J}_{SX}A\right) - m\ln\left(T\right)\right)\right). \tag{2.27}$$

The bandgap voltage appears as the first term on the right hand side of this equation.

Under the assumption that I_C is independent of temperature, differentiating (2.27) with respect to T gives

$$\frac{\partial V_{BE}}{\partial T} = \frac{k}{q}\left[\ln\left(\frac{I_C}{\tilde{I}_{SX}}\right) - m\left(1+\ln\left(T\right)\right)\right]. \tag{2.28}$$

Substituting (2.12) into (2.28) results in

$$\frac{\partial V_{BE}}{\partial T} = \frac{k}{q}\left[-m + \left(\frac{V_{BE}-V_{G0}}{V_T}\right)\right]. \tag{2.29}$$

At room temperature, this is approximately given by

$$\left.\frac{\partial V_{BE}}{\partial T}\right|_{T=T_0=300^\circ K} \cong 8.6\times10^{-5}\left[-2.3+\left(\frac{0.65-1.2}{25\times10^{-3}}\right)\right] \cong -2.1 mV/^\circ C\,. \qquad (2.30)$$

Although the collector current may not be constant or it may be difficult to maintain a constant collector current, if the current is relatively independent of temperature, V_{BE} will still have a negative temperature coefficient and the voltage value will depend substantially on the bandgap voltage. The V_{BE} voltage is usually used as the NTC voltage when designing voltage references following the approach described in Figure 2.1.

Consider now the difference of two base-emitter voltages. It follows from (2.17) that this can be expressed as

$$V_{BE2}-V_{BE1}=\Delta V_{BE}=\left[\frac{k}{q}\ln\left(\frac{J_{C2}}{J_{C1}}\right)\right]T\,. \qquad (2.31)$$

If the ratio of the two current densities is independent of temperature, then this difference is linearly proportional to temperature. If the ratio of current densities is larger than unity to make the natural logarithm of the ratio positive, then we say this voltage is Proportional To Absolute Temperature (PTAT) and the derivative is given by

$$\frac{\partial\left(V_{BE2}-V_{BE1}\right)}{\partial T}=\frac{k}{q}\ln\left(\frac{J_{C2}}{J_{C1}}\right). \qquad (2.32)$$

As an example, if the logarithmic function is 1, then at room temperature the PTAT voltage is

$$V_{BE2}-V_{BE1}=8.6\times10^{-5}\times300=25.8mV\,, \qquad (2.33)$$

and the derivative is

$$\left.\frac{\partial\left(V_{BE2}-V_{BE1}\right)}{\partial T}\right|_{T=T_0=300°K} = 8.6\times10^{-5} = 86\,\mu V/°C\,. \tag{2.34}$$

The PTAT voltage is often used to generate the PTC voltage in the bandgap circuits when designing voltage reference following the approach of Figure 2.1.

Voltage references using the architecture of Figure 2.1 with a circuit that presents ΔV_{BE} for the positive temperature coefficient block and the V_{BE} voltage for the negative temperature coefficient block are termed bandgap references. Even though ΔV_{BE} has a positive temperature coefficient, it is about a factor of 23 smaller than the negative temperature coefficient of V_{BE}, suggesting a large gain in (2.26) is needed to obtain a zero temperature coefficient if V_{BE} and ΔV_{BE} discussed above are used in the bandgap reference.

2.4 Characterization of Bandgap References

The circuit shown in Figure 2.2 is a widely used bandgap circuit that has been around since the mid 1970's [7] and is a circuit that is still widely used.

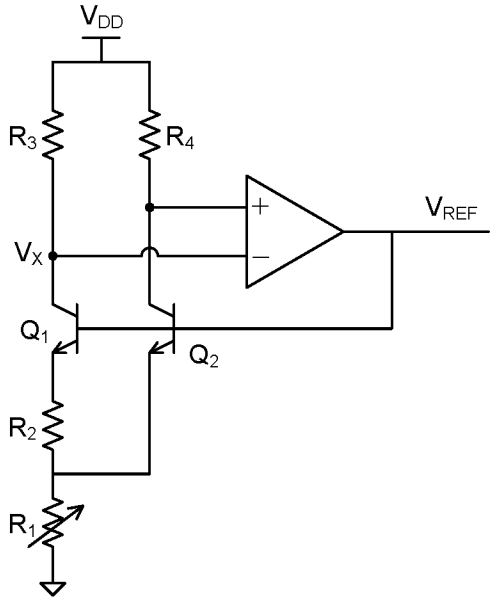

Figure 2.2 A typical bandgap circuit

Consider now the circuit shown in Figure 2.2. A routine analysis, under the assumption that the op amp has infinite gain yields the following set of equations

$$I_{E1}R_2 + V_{BE1} = V_{BE2} \tag{2.35}$$

$$V_{REF} = V_{BE2} + (I_{E1} + I_{E2})R_1 \tag{2.36}$$

$$I_{C1} = \frac{V_{DD} - V_{C2}}{R_3} \tag{2.37}$$

$$I_{C2} = \frac{V_{DD} - V_{C2}}{R_4} \tag{2.38}$$

The collector currents I_{C1} and I_{C2} relate to the emitter currents by the expressions

$$I_{C1} = \alpha_1 I_{E1} \tag{2.39}$$

$$I_{C2} = \alpha_2 I_{E2} \tag{2.40}$$

where the parameter α relates to β of the transistors by the expression

$$\alpha = \frac{\beta}{1+\beta} \tag{2.41}$$

Equations (2.35) through (2.40) constitute a set of 6 equations in the 8 unknowns $\{V_{REF}, V_{C2}, V_{BE1}, V_{BE2}, I_{C1}, I_{C2}, I_{E1}, I_{E2}\}$. Two additional equations are needed to obtain a complete set of independent equations that can be solved to obtain the voltage V_{REF}. These two equations are the I-V equations that characterize the two transistors Q_1 and Q_2. In the classical approach, the functional form of (2.4) is used for these two additional equations. In what we term the T_0-independent approach, the functional form of (2.14) is used for these two additional equations.

2.4.1 Standard T_0 Dependent Analysis

Following the standard approach, the two remaining device equations are

$$V_{BE1}(T) = V_{G0}\left(1-\frac{T}{T_0}\right) + V_{BE1}(T_0)\frac{T}{T_0} + \frac{mkT}{q}\ln\left(\frac{T_0}{T}\right) + \frac{kT}{q}\ln\left(\frac{J_{C1}(T)}{J_{C1}(T_0)}\right) \tag{2.42}$$

$$V_{BE2}(T) = V_{G0}\left(1-\frac{T}{T_0}\right) + V_{BE2}(T_0)\frac{T}{T_0} + \frac{mkT}{q}\ln\left(\frac{T_0}{T}\right) + \frac{kT}{q}\ln\left(\frac{J_{C2}(T)}{J_{C2}(T_0)}\right) \tag{2.43}$$

Solving equations (2.35)-(2.43) gives

$$V_{BE2} - V_{BE1} = \Delta V_{BE} = \left[\frac{k}{q}\ln\left(\frac{A_{E1}}{A_{E2}}\frac{R_3}{R_4}\right)\right]T. \tag{2.44}$$

Thus the voltage ΔV_{BE} is a PTAT voltage. It follows from (2.35)-(2.44) that

$$V_{REF} = V_{BE2} + \frac{R_1}{R_2}\left(1 + \left(\frac{\alpha_1}{\alpha_2}\right)\frac{R_3}{R_4}\right)\Delta V_{BE}. \tag{2.45}$$

Equation (2.45) shows that the reference voltage is the sum of terms that depend upon a V_{BE} voltage and a ΔV_{BE} voltage. This is an important relationship which provides the key functional relationship present in essentially all bandgap references.

Substituting for V_{BE2} and ΔV_{BE} from (2.43) and (2.44) into (2.45) gives the relationship

$$\begin{aligned} V_{REF} = &\left[V_{G0}\left(1 - \frac{T}{T_0}\right) + V_{BE2}(T_0)\frac{T}{T_0} + \frac{mkT}{q}\ln\left(\frac{T_0}{T}\right) + \frac{kT}{q}\ln\left(\frac{J_{C2}(T)}{J_{C2}(T_0)}\right)\right] \\ &+ \left\{\frac{R_1}{R_2}\left(1 + \frac{\alpha_1}{\alpha_2}\frac{R_3}{R_4}\right)\frac{k}{q}\ln\left(\frac{A_{E1}}{A_{E2}}\frac{R_3}{R_4}\right)\right\}T \end{aligned} \tag{2.46}$$

It follows from (2.35)-(2.41) that

$$I_{C2} = \alpha_1 \frac{R_3}{R_4}\frac{\Delta V_{BE}}{R_2} \tag{2.47}$$

Observe from (2.44) and (2.47) that I_{C2} is a PTAT current. Since the current ratios for Q_2 at two temperatures are equal to the current density ratios, it follows that

$$\frac{J_{C2}(T)}{J_{C2}(T_0)} = \frac{T}{T_0} \tag{2.48}$$

This can now be substituted into (2.46) to obtain

$$\begin{aligned} V_{REF}(T) = &V_{G0}\left(1 - \frac{T}{T_0}\right) + V_{BE2}(T_0)\frac{T}{T_0} + \frac{mkT}{q}\ln\left(\frac{T_0}{T}\right) \\ &+ \left\{\frac{R_1}{R_2}\left(1 + \frac{\alpha_1}{\alpha_2}\frac{R_3}{R_4}\right)\frac{k}{q}\ln\left(\frac{A_{E1}}{A_{E2}}\frac{R_3}{R_4}\right)\right\}T \end{aligned} \tag{2.49}$$

Equation (2.49) is where most authors stop in the analysis of the bandgap reference circuit but, unfortunately, it still contains the term $V_{BE2}(T_0)$ which is neither a model parameter nor a circuit parameter. We will now use (2.49) to obtain the inflection point following a classical analysis.

By definition, $V_{BE2}(T_0)$ is independent of temperature. Thus we can express V_{REF} in (2.49) as

$$V_{REF} = a + bT + cT\ln\frac{T_0}{T} \tag{2.50}$$

where

$$a = V_{G0} \tag{2.51}$$

$$b = -\frac{V_{G0}}{T_0} + \frac{V_{BE2}(T_0)}{T_0} + \frac{R_1}{R_2}\left(1 + \frac{\alpha_1}{\alpha_2}\frac{R_3}{R_4}\right)\frac{k}{q}\ln\left(\frac{A_{E1}}{A_{E2}}\frac{R_3}{R_4}\right) \tag{2.52}$$

$$c = \frac{(m-1)k}{q} \tag{2.53}$$

The parameters a, b and c are not dependent upon temperature. Differentiating V_{REF} with respect to T and setting it equal to 0 gives

$$\frac{dV_{REF}}{dT} = b + c\left(-1 + \ln\left(\frac{T_0}{T}\right)\right) = 0 \tag{2.54}$$

This expression can be solved for T to determine the inflection point T_{INF} as

$$T_{INF} = T_0 e^{\left(\frac{b}{c}-1\right)} \tag{2.55}$$

If we now want this derivative to be zero at T_0, it follows that $b = c$. To achieve this, the resistors must be trimmed so that

$$\frac{(m-1)k}{q} = -\frac{V_{G0}}{T_0} + \frac{V_{BE2}(T_0)}{T_0} + \frac{R_1}{R_2}\left(1 + \frac{\alpha_1}{\alpha_2}\frac{R_3}{R_4}\right)\frac{k}{q}\ln\left(\frac{A_{E1}}{A_{E2}}\frac{R_3}{R_4}\right) \tag{2.56}$$

And when this trim is made, it follows from (2.50) that

$$V_{REF} = a + cT\left(1 + \ln\frac{T_0}{T}\right) \tag{2.57}$$

or in terms of the circuit parameters

$$V_{REF} = V_{G0} + \frac{(m-1)k}{q}T\left(1 + \ln\frac{T_0}{T}\right) \tag{2.58}$$

However, the trim as required to meet the conditions in (2.56) is complicated by the fact that $V_{BE2}(T_0)$ is dependent upon the trim components themselves.

2.4.2 T_0 Independent Analysis

In this section the analysis will be repeated with complete removal of T_0 dependence. This is achieved by using the T_0-independent model of (2.14). By taking the natural logarithm of this model equation we obtain the model equations for Q_1 and Q_2 as follows

$$V_{BE1} = V_T \ln I_{C1} + \left[V_{G0} - V_T\left\{\ln\left(A_{E1}\tilde{J}_{SX}\right) + m\ln T\right\}\right] \tag{2.59}$$

$$V_{BE2} = V_T \ln I_{C2} + \left[V_{G0} - V_T\left\{\ln\left(A_{E2}\tilde{J}_{SX}\right) + m\ln T\right\}\right] \tag{2.60}$$

For convenience define the term in brackets to be the parameter $\tilde{\theta}$ so V_{BE} for the two transistors can be written as

$$V_{BE1} = V_T \ln I_{C1} + \tilde{\theta}_1 \tag{2.61}$$

$$V_{BE2} = V_T \ln I_{C2} + \tilde{\theta}_2 \tag{2.62}$$

where

$$\tilde{\theta}_1 = V_{G0} - V_T \left(\ln\left(A_{E1} \tilde{J}_{SX} \right) + m \ln T \right) \tag{2.63}$$

$$\tilde{\theta}_2 = V_{G0} - V_T \left(\ln\left(A_{E2} \tilde{J}_{SX} \right) + m \ln T \right) \tag{2.64}$$

The parameters $\tilde{\theta}_1$ and $\tilde{\theta}_2$ are dependent only on the device model and on temperature but are not dependent upon the circuit in which the device is used.

Following the same approach as used in the previous analysis, we can get

$$V_{BE2} - V_{BE1} = \Delta V_{BE} = \left[\frac{k}{q} \ln\left(\frac{A_{E1}}{A_{E2}} \frac{R_3}{R_4} \right) \right] T \tag{2.65}$$

and

$$V_{REF} = V_{BE2} + \frac{R_1}{R_2} \left(1 + \left(\frac{\alpha_1}{\alpha_2} \right) \frac{R_3}{R_4} \right) \Delta V_{BE} \tag{2.66}$$

which are the same as (2.44) and (2.45) obtained in the previous analysis. Solving (2.35)-(2.40) and (2.62) gives

$$V_{BE2} = V_T \ln\left(T \frac{k}{q} \frac{\alpha_1}{R_2} \frac{R_3}{R_4} \ln\left(\frac{A_{E1}}{A_{E2}} \frac{R_3}{R_4} \right) \right) + \tilde{\theta}_2 \tag{2.67}$$

Substituting from (2.64) for $\tilde{\theta}_2$ into (2.67) gives

$$V_{BE2} = V_{G0} + (1-m)V_T \ln T + V_T \ln\left(\frac{k}{q}\frac{\alpha_1}{R_2 A_{E2}\tilde{J}_{SX}}\frac{R_3}{R_4}\ln\left(\frac{A_{E1}}{A_{E2}}\frac{R_3}{R_4}\right)\right) \tag{2.68}$$

Substituting (2.68) and (2.65) into (2.66) we obtain the expression for V_{REF}

$$\begin{aligned} V_{REF} = {} & V_T \ln\left\{\frac{\alpha_1}{R_2}\frac{R_3}{R_4}T\frac{k}{q}\ln\left(\frac{A_{E1}}{A_{E2}}\frac{R_3}{R_\$}\right)\right\} + V_{G0} - V_T\left(\ln\left(\tilde{I}_{SX2}\right) + m\ln T\right) \\ & + \left[\frac{k}{q}\ln\left(\frac{A_{E1}}{A_{E2}}\left(\frac{R_3}{R_4}\right)\right)\right]\left[\frac{R_1}{R_2}\left(1+\frac{\alpha_1}{\alpha_2}\frac{R_3}{R_4}\right)\right]T \end{aligned} \tag{2.69}$$

Although this equation is more involved than (2.49), it can be observed that T_0 dependence and V_{BE} dependence have been completely removed and, more importantly, it is a closed-form explicit expression that involves only circuit and model parameters. With some manipulations, (2.69) can be expressed as

$$V_{REF} = a_1 + b_1 T + c_1 T \ln T \tag{2.70}$$

where

$$a_1 = V_{G0} \tag{2.71}$$

$$b_1 = \frac{k}{q}\left(\frac{R_1}{R_2}\left(1+\frac{\alpha_1}{\alpha_2}\frac{R_3}{R_4}\right)\ln\left(\frac{A_{E1}}{A_{E2}}\frac{R_3}{R_4}\right) + \ln\left(\frac{k}{q}\frac{R_3}{R_4}\alpha_1\frac{\ln\left(\frac{R_3}{R_4}\frac{A_{E1}}{A_{E2}}\right)}{\tilde{I}_{SX2}R_2}\right)\right) \tag{2.72}$$

$$c_1 = \frac{k}{q}(1-m) \tag{2.73}$$

When written in this form, the parameters a_1, b_1 and c_1 are model and circuit parameters and are independent of temperature.

The inflection point can be readily calculated from (2.70) by taking the derivative of V_{REF} with respect to T to obtain

$$\frac{dV_{REF}}{dT} = b_1 + c_1(1 + \ln T) = 0 \tag{2.74}$$

If b_1 and c_1 are fixed, this can be solved for T to obtain the inflection point

$$T_{INF} = e^{-\left(1+\frac{b_1}{c_1}\right)} \tag{2.75}$$

If the desired T_{INF} is fixed, then it follows from (2.75) that the resistor values in the expression for b_1 must be set so that

$$b_1 = -c_1(1 + \ln T_{INF}) \tag{2.76}$$

Substituting this expression for b_1 back into (2.70) we obtain an expression for the reference voltage at the T_{INF} as

$$V_{REF} = a_1 - c_1 T_{INF} \tag{2.77}$$

Substituting for a_1 and c_1 from (2.71) and (2.73) we obtain the value for V_{REF} at the inflection point to be

$$V_{REF} = V_{G0} + \frac{kT_{INF}}{q}(m-1) \tag{2.78}$$

Note that V_{REF} is completely determined by the inflection point location and the resistors in the network can not be used to adjust V_{REF}.

If the inflection point is placed at the desired operating temperature, T_{INF}, then different references can be compared by considering how rapidly they open up way from the

inflection point. A good measure of this is the second derivative of the reference voltage evaluated at the inflection point. It follows from (2.74) that

$$\left.\frac{\partial^2 V_{REF}}{\partial T^2}\right|_{T=T_{INF}} = \frac{c_1}{T_{INF}} \tag{2.79}$$

Equation (2.79) shows that the second derivative of the output voltage is independent of circuit parameters assuming perfect matching and ideal op amp.

2.5 Conclusion

Characteristics of bandgap references are explored and analyzed. Instead of the commonly used V_{BE} involved approximate expression of the reference voltage output, an explicit close-form expression which is only dependent on process and model parameters are derived based on accurate modeling of bandgap references. This work helps better understanding of the bandgap references and inspiration of new bandgap reference design techniques.

CHAPTER 3 A COST-EFFECTIVE HISTOGRAM TEST-BASED ALGORITHM FOR DIGITAL CALIBRATION OF HIGH-PRECISION PIPELINE ADCS

In this work, a self-calibration algorithm that corrects the linearity errors of pipeline ADCs with a sub-radix architecture, based on the results of simple code density tests, is presented. The proposed algorithm identifies discontinuities in an ADC's output histogram data, calculates correction codes for transitions in pipeline stages, and digitally calibrates the ADC's output codes. Simulation results show that the calibration can dramatically improve the linearity performance of ADCs. With this approach, the INL can be reduced from about 1000 LSB in a sample uncalibrated ADC to less than 1 LSB in the calibrated ADC. Since this algorithm is based on conventional code density tests and uses only a few memory cells and simple logic circuits to carry out the calibration, this algorithm can be easily implemented on chip without requiring much area and the associated cost overhead. It also serves as a self-calibration solution for high-speed high-precision pipeline ADCs.

3.1 Introduction

The pipeline architecture is widely used in high speed, high resolution analog-to-digital converter (ADC) design. Particularly, the 1b/stage and 1.5b/stage pipeline configurations with over range protection are often used, because each stage has a very simple structure and is relatively easy to implement. However, issues like capacitor mismatch, comparator offset, charge injection, and finite gain and nonlinearity of op amps all limit the

accuracy of ADC stages. Handling these issues directly is not favorable or even not doable. For example, the capacitor mismatch or comparator offset can only be reduced at the cost of large area consumption and it is impossible to achieve infinite or completely linear op amp gain.

Over the years, great efforts have been made on improving the performance of pipeline ADCs. Error averaging [14] and analog calibration [15] techniques have been proposed but these techniques require elaborate calibration schemes and complex additional circuits which greatly increase the difficulty of circuit design. As compared to analog calibration, digital calibration offers some advantages because it is often simpler to implement, it often provides lower complexity, and it often consumes less area. Soenen and Geiger proposed an algorithm and architecture for digitally calibrating pipeline ADCs [16]. The circuit and the calibration scheme were so designed that the same hardware used in the calibration mode was used in the conversion mode. Karanicolas, Lee, and Bacrania also gave a simpler ADC architecture with an applicable digital self-calibration scheme [17]. All the previously reported digital calibration schemes inevitably require modification of the internal pipeline stages to allow external control during the calibration phase. This is not attractive, in part, because calibration which requires disturbance of the pipeline may introduce errors into the pipeline itself, especially when the ADC's resolution is high. Reuse of such calibration algorithms is difficult as well since architecture-specific calibrations are not applicable to ADCs with different architectures.

In this work, a new algorithm for digitally calibrating pipeline ADCs is introduced. The calibration algorithm is based on results of input-output histogram tests so that it does not disturb the data path of an ADC during test and does not require external control of the

pipeline stages. Correction codes are calculated from the discontinuities in the histogram data. This digital calibration can be done with a small number of memory elements, a digital adder, and some simple control logic blocks. Furthermore, this algorithm does not require a precision ramp or any other precision signal for the input of the histogram test. All these features make this algorithm applicable for on-chip implementations. Simulations show that the INL of an example ADC can be reduced from about 1000 LSB originally to less than 1 LSB after calibration, which is comparable to what the algorithm reported in [17] can achieve for nominally the same structure.

The term "histogram test" has been used above and will be used throughout this chapter. To avoid possible confusion between the use of this term and use of the term "histogram test" in conventional production testing for INL measurements, some comments about this term in the context of the proposed calibration algorithm are in order. In the context of this thesis, a "histogram test" refers to generating a set of histogram data by applying a test signal to the input of the ADC. The requirements on the test signal are not critical and, in particular, have very lax requirements on linearity. Beyond providing inputs that excite all output codes modestly uniformly, there are few other requirements on the test signal. As such, the histogram data does not contain sufficient information to "test" the linearity of the ADC. It does, however, contain sufficient information to identify void code ranges and it is this information that is needed to calibrate the ADC. We refer to this generation of histogram data for the purpose of identifying void code ranges as a "histogram test".

The rest of the chapter is organized as follows. In Section 3.2, the pipeline architecture is reviewed and a mathematical formulation of the pipeline data converter is

presented. The principle of the digital calibration algorithm is developed in Section 3.3. Implementation issues and simulation results appear in Sections 3.4 and 3.5 respectively. A conclusion of the work is presented in Section 3.6.

3.2 Pipeline Architecture and Modeling

A1-bit/stage pipeline architecture is shown in Figure 3.1. A sample and hold stage is not shown in the figure but is usually needed in front of the pipeline to hold the input voltage when the 1st stage is doing conversion and the Vin in Figure 3.1 actually comes from the output of the sample and hold stage. For each stage, the comparator compares the input voltage with 0, and gives a 1-bit digital output. The output voltage of the stage is determined by the input voltage and the comparator output, which can be described as follows.

For any pipeline stage k, k=1, 2, 3…

$$d_k = \begin{cases} 0 & V_{ink} < 0 \\ 1 & V_{ink} > 0 \end{cases} \tag{3.1}$$

$$V_{outk} = 2 \times \left[V_{ink} + \frac{V_{ref}}{2} - V_{ref} \times d_k \right] \tag{3.2}$$

where V_{ink} and V_{outk} are the input and output voltages of stage k, respectively; d_k is the 1-bit digital output of stage k; and V_{ref} is the reference voltage.

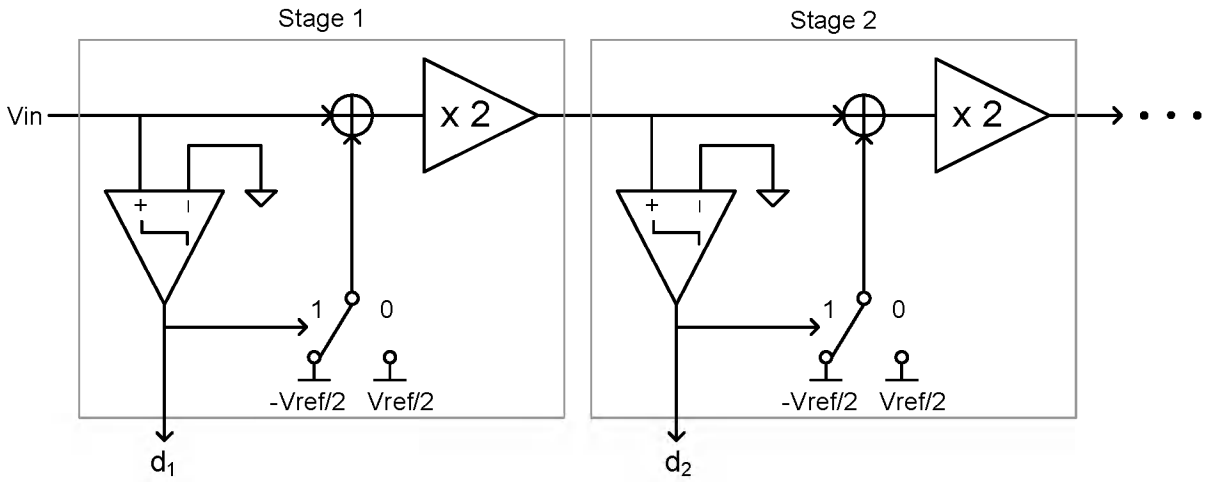

Figure 3.1 A pipeline ADC architecture with 1 bit/stage resolution

Due to issues such as capacitor mismatch, charge injection, comparator offset, and finite op amp gain, the output voltage of one stage may exceed the input range of the next stage, which will cause missing decision levels. This over-range problem can be avoided by intentionally setting the nominal gain of each stage to be less than 2 [17].

A modified pipeline ADC with one comparator per stage is shown in Figure 3.2. Although an actual implementation will often combine the gain blocks and summer into a single summing/amplifier block, it is useful for modeling a pipeline ADC. The comparator output that controls the two switches along with the gain blocks and summer and the two voltage sources V_{r1k} and V_{r2k} in each stage comprises a 1-bit DAC. In this structure the gain in the signal path is g_{11}, g_{12}, ….g_{1n}, where n is the number of stages. In a practical implementation, the gain and summer blocks and the DAC in the last stage are generally not included. The reference voltages are designated as V_{r1k} and V_{r2k} for k=1,2,…n and the gains g_{21}, g_{22}, ..g_{2n} represent the gains from the DAC outputs in the corresponding stages. If the signal path gains are all the same and equal to g_1, this is termed a "radix g_1" structure. Thus,

the example in Figure 3.1 is termed a radix 2 structure. If the radix is less than 2, it is often termed a sub-radix structure.

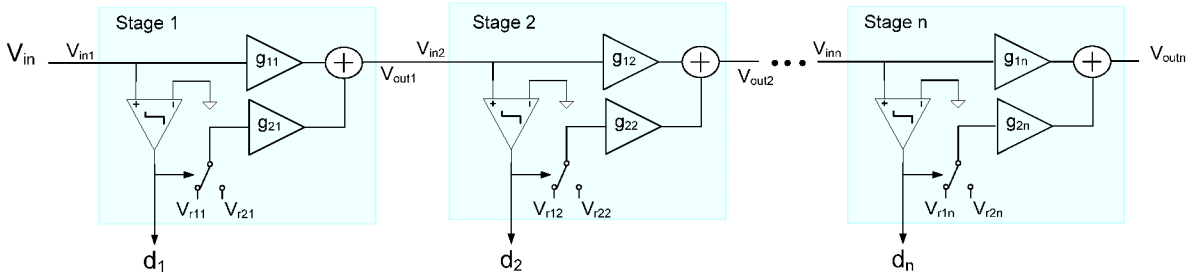

Figure 3.2 Block diagram of one comparator/stage pipeline architecture

The modified ideal transfer characteristics of one stage of the more general pipeline architecture are shown in Figure 3.3(a). With an appropriate reduction of the signal path gain below the value of 2, the output voltage of every stage can be assured to be within the input range of the next stage even in the presence of errors such as capacitor mismatch and comparator offset. With such sub-radix structures, a pipeline comprised of n stages will not provide 2^n digital output codes and thus will not provide n bit resolution. To compensate for this loss in resolution, additional pipeline stages can be added to provide enough redundancy in decision levels to resolve 2^n distinct signal levels. The sub-radix structures will have missing codes in the output causing gaps or void ranges in the digital output codes. These gaps are necessary to provide over-range protection in the presence of process variations and the width of the gaps will change with the random variations of the gains and offset voltages in the pipeline ADC. If uncorrected, these gaps or void ranges cause unreasonably large INL and DNL. With calibration, these gaps in the output code can be removed.

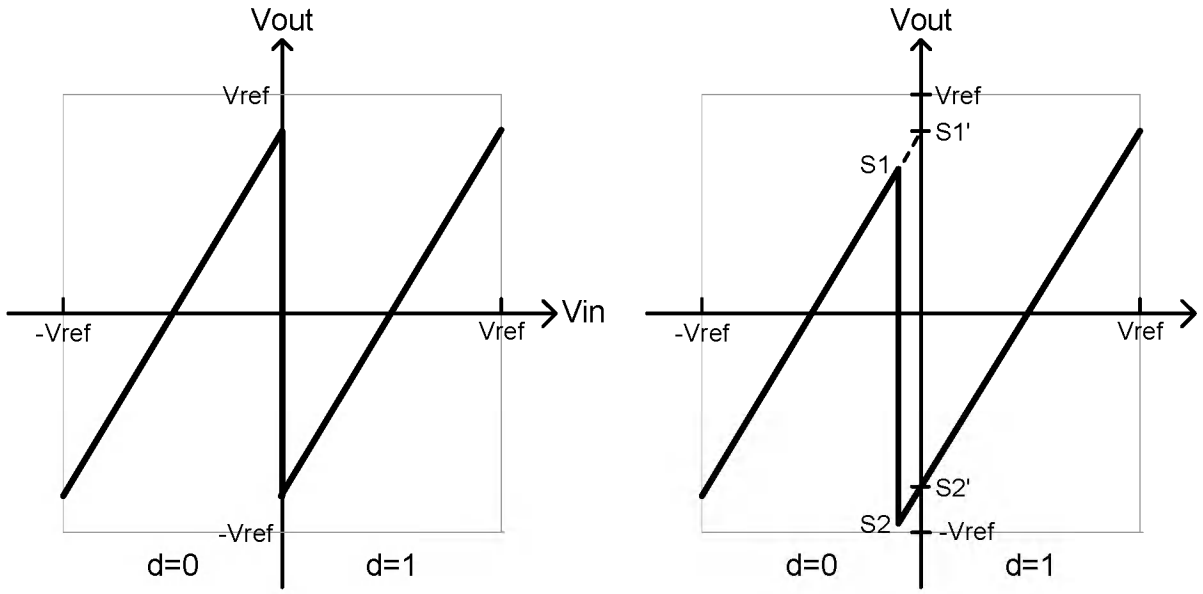

Figure 3.3 Ideal and actual transfer curve of a sub-radix pipeline stage

A mathematical model of a one comparator/stage pipeline ADC with over-range protection obtained by using a sub-radix approach with extra pipeline stages will now be developed. In this model, it will be assumed that all stages are nominally the same and the target resolution after calibration is m bits where m<n. The nominal gains and DAC levels will be denoted as g_{1NOM}, g_{2NOM}, V_{r1NOM} and V_{r2NOM}. The offset voltage of the comparator of stage k is denoted as V_{osk}. Suppose for each pipeline stage

1) The nominal value of the DAC gain is ½ that of the signal path gain, i.e. $g_{2kNOM}=g_{1kNOM}/2$. As an example, we will set the nominal values to be $g_{1NOM}=1.93$ and $g_{2NOM}=0.965$;

2) The comparator has an offset with nominal value $V_{osNOM}=0$;

3) The nominal values of the reference voltages V_{r1NOM} and V_{r2NOM} are $-V_{ref}$ and $+V_{ref}$, respectively.

The comparator as well as the two amplifiers generally are adversely affected by a random input-referred offset voltage. Since a regenerative comparator that is noted for a rather high offset voltage is often used for the comparator, this offset voltage will be included in this formulation. The offset voltage of the amplifiers will be neglected for notational convenience but inclusion of the amplifier offset voltage does not fundamentally affect the approach used to model the pipeline stages. With these assumptions and an assumption that the amplifiers are linear, the transfer characteristics of stage k can be expressed as

$$V_{outk} = \begin{cases} g_{1k} \cdot V_{ink} - g_{2k} \cdot V_{r1k} & d_k = 0 \\ g_{1k} \cdot V_{ink} - g_{2k} \cdot V_{r2k} & d_k = 1 \end{cases}, \tag{3.3}$$

where

$$d_k = \begin{cases} 0 & V_{in\,k} < V_{os\,k} \\ 1 & V_{in\,k} > V_{os\,k} \end{cases}. \tag{3.4}$$

Solving for V_{ink} from (3.3) and (3.4) gives

$$V_{ink} = \frac{V_{outk}}{g_{1k}} + \frac{g_{2k}}{g_{1k}} V_{r1k} + d_k \frac{g_{2k}}{g_{1k}} \left(V_{r\,2k} - V_{r1k} \right). \tag{3.5}$$

For the 1st stage, we get

$$V_{in} = \frac{V_{out1}}{g_{11}} + \frac{g_{21}}{g_{11}} V_{r11} + d_1 \frac{g_{21}}{g_{11}} \left(V_{r\,21} - V_{r11} \right). \tag{3.6}$$

Since the 1st stage's output is also the 2nd stage's input,

$$V_{out1} = V_{in\,2} = \frac{V_{out2}}{g_{12}} + \frac{g_{22}}{g_{12}} V_{r12} + d_2 \frac{g_{22}}{g_{12}} \left(V_{r22} - V_{r12} \right). \tag{3.7}$$

Substituting (3.7) to (3.6) and doing this iteratively for all the n stages gives

$$V_{in} = \sum_{i=1}^{n} d_i \frac{g_{2i}}{\prod_{j=1}^{i} g_{1j}} (V_{r2i} - V_{r1i}) + \sum_{i=1}^{n} \frac{g_{2i}}{\prod_{j=1}^{i} g_{1j}} V_{r1i} + \frac{V_{outn}}{\prod_{i=1}^{n} g_{1i}}. \quad (3.8)$$

The last term on the right hand side of (3.8) is the residue of the last stage, which is always less than 1/2 LSB and is the quantization error of the ADC. The second term is a constant offset. The first term is the most important one, which shows that V_{in} can be accurately interpreted (up to n bit resolution) from the digital output as long as $g_{2i}(V_{r2i} - V_{r1i}) \Big/ \prod_{j=1}^{i} g_{1j}$ is known for all stages.

3.3 Digital Calibration Algorithm

A digital calibration algorithm will now be developed. By neglecting the last term in (3.8) and multiplying the two sides by $\prod_{i=1}^{n} g_{1i} \Big/ 2V_{ref}$, a normalized estimate for V_{in}, denoted as $\hat{V}_{in}$, can be obtained. This can be expressed as

$$\hat{V}_{in} = \sum_{i=1}^{n} d_i w_i + C, \quad (3.9)$$

where

$$w_i = g_{2i} \prod_{j=i+1}^{n} g_{1j} \frac{V_{r2i} - V_{r1i}}{2V_{ref}} \quad (3.10)$$

and

$$C = \sum_{i=1}^{n} \left(g_{2i} \prod_{j=i+1}^{n} g_{1j} \frac{V_{r1i}}{2V_{ref}} \right). \quad (3.11)$$

Since $\hat{V}_{in}$ is a normalized estimation of V_{in}, it should have the same linearity performance as V_{in}. If we interpret the digital output using powers of 2, essentially we are assuming g_{1i}=2 and g_{2i}=1, and V_{r2i}-V_{r1i}=2V_{ref} for all *i*'s, then (3.9) becomes

$$\hat{V}'_{in} = \sum_{i=1}^{n} d_i 2^{n-i} - \sum_{i=1}^{n} 2^{n-i-1} \quad . \tag{3.12}$$

Comparing (3.9)~(3.11) with (3.12), we can see that for the sub-radix configuration since the gain is intentionally set to be less than 2, the actual value of w_i is less than 2^{n-i}. If the sub-radix approach is to be effective at providing over-range protection, the nominal gain, at least in the earlier stages, must be reduced enough to cause gaps (alt discontinuities) in the output codes even under worst-case parametric variations, that is, codes which will not appear as an output of the ADC for any input. Calibration requires removal of the discontinuities.

To remove the discontinuities in the output codes, a good estimation of the w_i*'s* is needed. Direct measurement of parameters such as g_i, V_{r1i} and V_{r2i} is infeasible. Fortunately, there exist digital calibration algorithms that can effectively calculate w_i without knowing the exact value of these parameters. The algorithm proposed in [17] tried to measure the jump in the transfer curve (S1-S2 in Figure 3.3(b)) of each stage, which is essentially w_i. However, there are two potential problems associated with this algorithm. First, the algorithm actually doesn't measure S1-S2, it measures S1'-S2' shown in Figure 3.3(b) instead. Because of the nonlinearity of the op amp, S1-S2 and S1'-S2' may not be the same and this will become more problematic when the ADC's resolution increases. Second, the pipeline is interrupted and externally controlled when implementing the calibration algorithm of [17], which means

the pipeline in the calibration mode may not be the same as that in conversion mode. Thus the correction code may not accurately represent the pipeline working in the conversion mode.

A method for identifying the missing output codes will now be presented. We term this procedure the "histogram test". The calibration algorithm will be developed from knowledge of which output codes are present and which output codes are missing when input signals that span the input range are applied. To determine the missing output codes, we will excite the input with a continuous-time input signal that spans the input range. The input should extend a little above and a little below the nominal input range. This input signal might be a "ramp-like" signal although other input signals can be used. Code density information will be generated, specifically we will record which code bins have been excited and how often they are excited. The average number of samples per code bin is not critical since we are interested only in finding the gaps in the output codes and thus linearity of the input signal is of little concern. An input signal that provides an average of somewhere 20 samples per non-empty code bin should be adequate. If plotted as a function of the raw digital output code, the histogram will have some ranges of consecutive codes with nonempty bins and other ranges of consecutive codes with empty bins. For notational convenience, we will refer to those ranges corresponding to empty bins as "gaps" and those ranges corresponding to non-empty bins as "code intervals". Thus, the histogram information could be viewed as a sequence of alternating code intervals and gaps with varying lengths for the code intervals and gaps.

Figure 3.4 illustrates how the sub-radix structure affects the output histogram of an ADC. In Figure 3.4, the dashed line represents the overall transfer curve of an ideal ADC

with infinite resolution. If the first stage of that ADC uses a sub-radix structure instead, then the transfer curve will look like the solid line in Figure 3.4. Notice that there is a jump at about the middle of the transfer curve caused by the sub-radix structure, meaning that Vout is discontinuous. If in reality the ADC has 4 bit resolution, then for any Vin, the corresponding Vout according to the transfer curve must be quantized to fit into one of the 16 code bins. When doing histogram test, for a transfer curve like the dashed line in Figure 3.4, all the code bins will have similar counts. For a transfer curve like the solid line in Figure 3.4, a lot of code bins still have similar counts (codes 1-5,10-13 in Figure 3.4). There will also be code bins with 0 count (codes 0,7,8,15 in Figure 3.4), which we call "missing codes" and code bins where counts are >0 but smaller than other codes that are not missing (codes 6,9,14 in Figure 3.4) because the transfer curve is discontinuous and does not cover the whole output range corresponding to that code bin and these codes will only happen at the two boundaries between missing codes and unmissing codes.

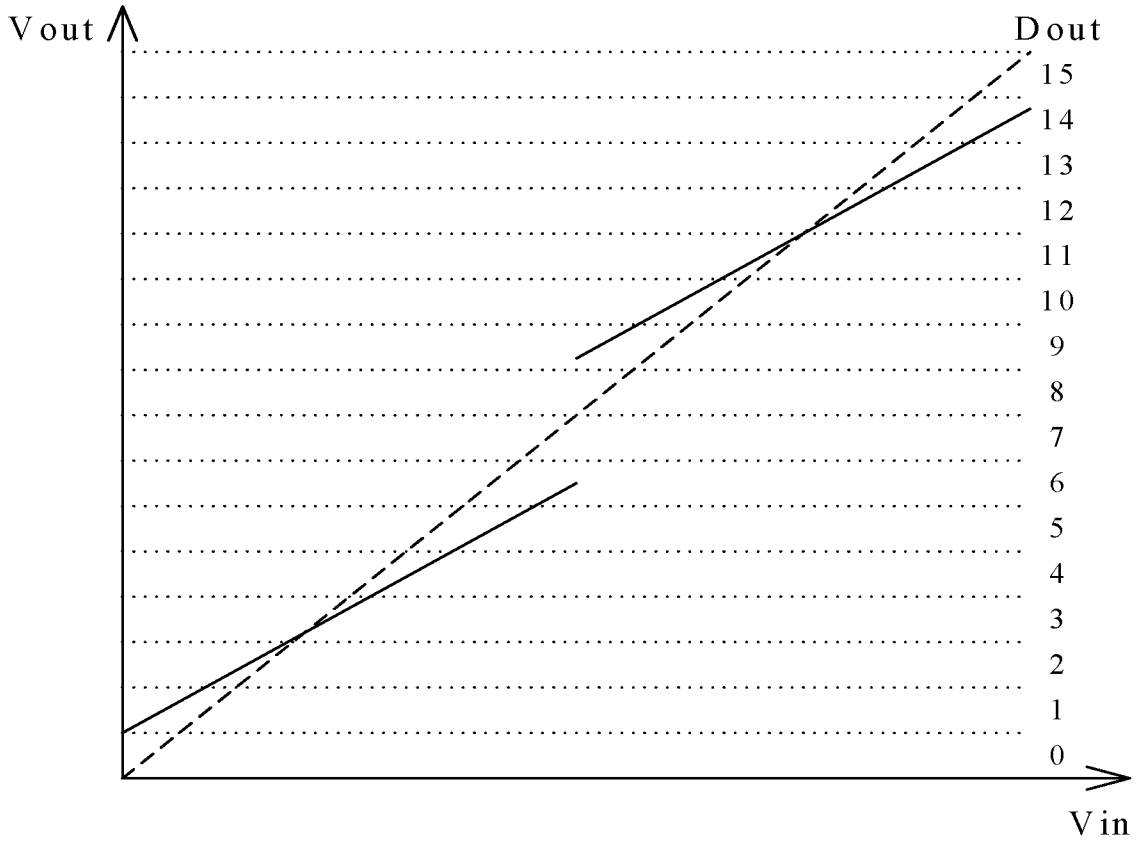

Figure 3.4 ADC's transfer curve with a sub-radix 1st stage

Looking at the discontinuity problem from another viewpoint may now give us more insight about the relationship between the output codes and ADC characteristics. Notice that the discontinuities in the output codes show up as gaps composed of empty bins in the output histogram obtained from the histogram test. The gap's width is the difference between ADC's two outputs for two very closely spaced inputs. When using the digital output code to represent the input signal, there should be no gaps in the digital output code since inputs used to generate the histogram data should result in consecutive output codes. If all code bins that are not empty have approximately the same number of hits from the histogram test, the corrected output code corresponding to any output code should be the summation of the widths of all code intervals that are present before the output code plus the number of

elements in the current code interval that are less than or equal to the current output code. Because of quantization effects, the number of elements in code bins on the edges of the code intervals may be only partially full. Bins that are only partially full on the edges of code intervals will be either treated as empty bins or full bins, depending upon how full the bin is relative to the average number of elements in the bins internal to the code intervals. With this provision for handling the partially full bins on the edges of the code intervals, a modified histogram is obtained. With the modified histogram, we can now formalize a calibration strategy.

Histogram-Test Based Calibration Strategy

If D_k is the raw output code for the ADC that is part of a code interval in the modified histogram , the calibrated value for code D_k is equal to the sum of the length of all code intervals corresponding to codes less than D_k plus the number of elements in the code interval for code D_k that are less than or equal to *code D_k where the code intervals are determined from the modified histogram. If D_k is not a part of a code interval in the modified histogram, then either D_{k-1} or D_{k+1} is a part of a code interval in the modified histogram and the calibrated value of D_k is equal to the calibrated value of D_{k-1} or D_{k+1} depending on which one is a part of a code interval in the modified histogram.*

Although conceptually straightforward, a direct implementation of this calibration strategy is difficult because storing a correction code for each output code requires too much memory if n is very large. When the nominal gain is set to be less than two, (3.9)~(3.12) show that the difference between $\hat{V}'_{in}$ and $\hat{V}_{in}$ is caused by the difference between w_i and 2^{n-i} in each stage i whose digital output d_i=1, excluding a constant offset.

If D_i is an output code, and D_{ic} is the calibrated value of D_i, then D_i can be related to the code D_{ic} by a correction code c_i as given by the equation

$$D_{ic} = D_i - c_i . \tag{3.13}$$

It can be observed that the correction code can be viewed as a quantization of $\hat{V}'_{in} - \hat{V}_{in}$ which can be thought of as a linear combination of the correction codes coming from each of the stages plus an offset. That is to say, if we can find a group of correction codes corresponding to the w_i-2^{n-i} of each stage (each bit), defined as

$$\boldsymbol{c}_b = \begin{pmatrix} c_{b1} & c_{b2} & \cdots & c_{bn} \end{pmatrix}^T , \tag{3.14}$$

then the correction codes c_i for a specific output code D_i can be estimated by adding up the bit correction codes corresponding to those stages whose digital output is 1, plus the offset. That is

$$c_i = \boldsymbol{D}_i \times \boldsymbol{c}_b + c_{os} , \tag{3.15}$$

where

$$\boldsymbol{D}_i = \begin{pmatrix} d_{1i} & d_{2i} & \cdots & d_{ni} \end{pmatrix} . \tag{3.16}$$

A method for obtaining $\boldsymbol{c}_b$ and c_{os} will now be developed. Given the modified output histogram obtained from the histogram test, for any output code D_i that is in a code interval, the correction code c_i can be calculated from the Histogram-based Calibration by summing the code interval widths up to obtain D_{ic} and then use equation (3.13) to obtain

$$c_i = D_i - D_{ic} . \tag{3.17}$$

The goal is thus to estimate $\boldsymbol{c}_{bit}$ in the following equation

$$\boldsymbol{D} \times \boldsymbol{c}_{bit} = \boldsymbol{C} \tag{3.18}$$

where

$$\boldsymbol{D} = \begin{pmatrix} \boldsymbol{D}_1 & 1 \\ \boldsymbol{D}_2 & 1 \\ \vdots & \vdots \\ \boldsymbol{D}_N & 1 \end{pmatrix} = \begin{pmatrix} \mathrm{d}_{11} & \mathrm{d}_{21} & \cdots & \mathrm{d}_{\mathrm{n}1} & 1 \\ \mathrm{d}_{12} & \mathrm{d}_{22} & \cdots & \mathrm{d}_{\mathrm{n}2} & 1 \\ \vdots & \vdots & \ddots & \vdots & \vdots \\ \mathrm{d}_{1\mathrm{N}} & \mathrm{d}_{2\mathrm{N}} & \cdots & \mathrm{d}_{\mathrm{nN}} & 1 \end{pmatrix}, \tag{3.19}$$

$$\boldsymbol{c}_{bit} = \begin{pmatrix} c_{b1} & c_{b2} & \cdots & c_{b\mathrm{n}} & c_{os} \end{pmatrix}^T, \tag{3.20}$$

$$\boldsymbol{C} = \begin{pmatrix} c_1 & c_2 & \cdots & c_{\mathrm{N}} \end{pmatrix}^T, \tag{3.21}$$

and N is the total number of output codes in the code intervals of the modified histogram. Last column in $\boldsymbol{D}$ and last element in $\boldsymbol{c}_{bit}$ was used for correcting the offset.

We will now minimize the mean-squared error of the difference between the calculated correction code and that predicted by the $\boldsymbol{D} \times \hat{\boldsymbol{c}}_{bit}$ with respect to the n+1 elements in $\hat{\boldsymbol{c}}_{bit}$. $\hat{\boldsymbol{c}}_{bit}$ should be chosen as

$$\hat{\boldsymbol{c}}_{bit} = \arg\min_{\boldsymbol{c}} \left\| \boldsymbol{C} - \boldsymbol{D} \times \boldsymbol{c} \right\|^2 \tag{3.22}$$

Solving $\dfrac{\partial \left\| \boldsymbol{C} - \boldsymbol{D} \times \boldsymbol{c} \right\|^2}{\partial \boldsymbol{c}} = 0$ gives

$$\hat{\boldsymbol{c}}_{bit} = \left(\boldsymbol{D}^T \boldsymbol{D} \right)^{-1} \boldsymbol{D}^T \boldsymbol{C} = \boldsymbol{D}^{+} \boldsymbol{C} \tag{3.23}$$

where $\boldsymbol{D}^{+}$ is the pseudo inverse of matrix $\boldsymbol{D}$. Given the output histogram, $\boldsymbol{D}$ and $\boldsymbol{C}$ can be easily obtained and applying (3.23) will directly give $\hat{\boldsymbol{c}}_{bit}$, which is the correction code for

each stage and the offset. After $\hat{\boldsymbol{c}}_{bit}$ is obtained, for any digital output $\boldsymbol{D}_i$, the corresponding correction code $\hat{c}_i$ can be calculated as

$$\hat{c}_i = \left(\boldsymbol{D}_i \quad 1\right) \times \hat{\boldsymbol{c}}_{bit} \tag{3.24}$$

3.4 Implementation and Performance Issues

Equation (3.24) shows that instead of storing a correction code for each output code, we only need to store a small group of correction codes corresponding to each pipeline stage and an offset. The correction code for a particular output code can be easily calculated from $\hat{\boldsymbol{c}}_{bit}$. As a result, when implementing the digital correction on-chip, the memory requirement is dramatically reduced (from the order of 2^n to that of n, where n is the number of stages). And only an adder is needed for calculating the correction code of a digital output.

However, according the formulation described above, the calculation of $\hat{\boldsymbol{c}}_{bit}$ from the histogram data needs to be done off-chip. How to implement this part on-chip is out of the focus of this work but some thoughts are given here. Since there are only (n+1) unknowns in $\hat{\boldsymbol{c}}_{bit}$ to be solved, there is a lot of redundancy in ADC's histogram data. Suspects are that only a small subset of the histogram data is needed while still resulting in a rather accurate estimation of $\boldsymbol{c}_{bit}$. If this can be done, then the algorithm should be able to be totally implemented on-chip without too much hardware overhead.

Since $\hat{\boldsymbol{c}}_{bit}$ is calculated based on $\boldsymbol{D}$ and $\boldsymbol{C}$, which are obtained from the histogram test, no interruption of the internal residue path of each pipeline stage is needed. The pipeline is exactly the same in the calibration mode as in the conversion mode. And since the algorithm uses the digital output, which changes when the input pass the trip point of the comparator,

the algorithm should give a better estimation of the voltage jump in the transfer curve than the algorithm proposed in [17].

3.5 Simulation Results

The calibration algorithm has been applied to a 15-bit pipeline ADC in a MATLAB simulation. The pipeline is comprised of 17 stages, and each stage provides a 1-bit output. The nominal gains of the first 11 stages were set to be 1.93 and the nominal gains of the remaining 6 stages were set to 2 while each stage's gain is randomized with some standard deviation. For each stage, the comparator offset has a nominal value of 0 and Vref has a nominal value of 1V while all of these are also randomized with some standard deviation. The last two bits were truncated after calibration to give a 15-bit digital output.

Figure 3.5 shows the nonlinearity of a typical sample ADC considered in these simulations before calibration. Figure 3.6 and Figure 3.7 show the calibrated nonlinearity of the ADC after applying the algorithm proposed in this thesis and in [17], respectively. The un-calibrated ADC has a peak INL of about 1000 LSB at the 17 bit level. However, the large INL is caused by the gaps in the output codes introduced by the sub-radix architecture for the over-range protection purpose and hence does not represent the true nonlinearity of the ADC. It should be clarified that Figure 3.5 is a plot of INL_k vs. the interpreted output code of the ADC. For codes that are missing, INL_k is not well defined. However, the plotter used to generate the plot tends to connect all the points in sequence. As a result, the INL_k in Figure 3.5 for the missing codes are not true INL_k but caused by interpolation of the two adjacent well-defined INL_k's by the plotter and no real INL_k data was there. After eliminating the discontinuities in the output codes, as shown in Figure 3.6, the proposed algorithm reduces

the INL to be less than 1 LSB and DNL is about 0.3 LSB after calibration, which is comparable to the result of applying the algorithm proposed in [17], which is about 1 LSB INL and 0.5 LSB DNL as shown in Figure 3.7.

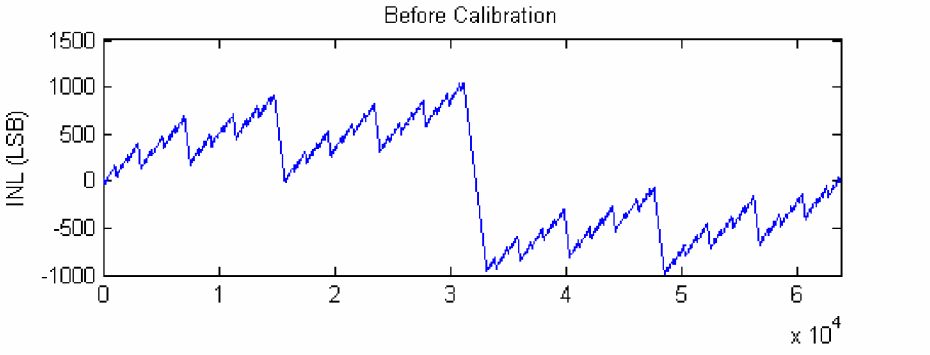

Figure 3.5 ADC's linearity before calibration

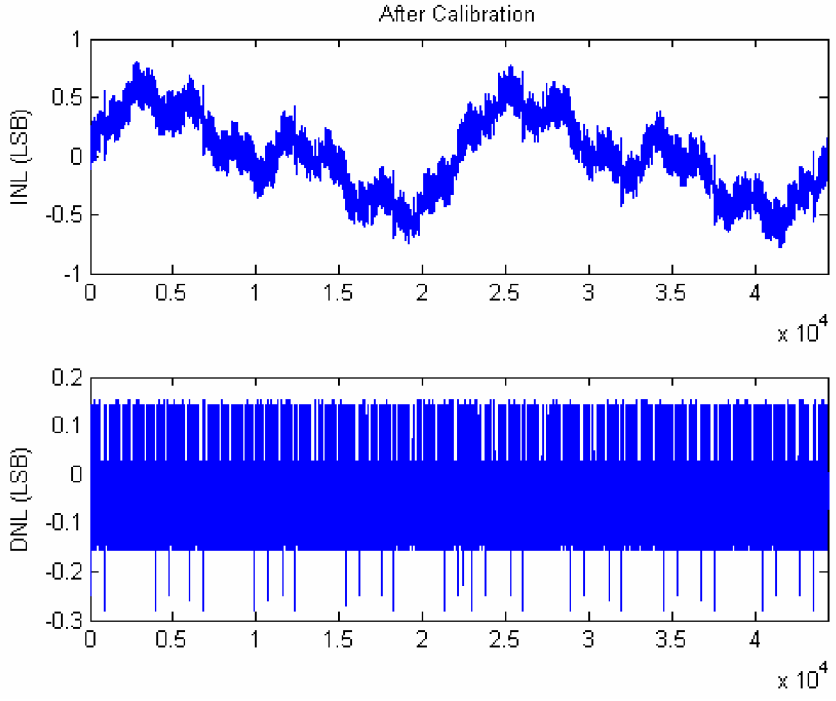

Figure 3.6 ADC's linearity after calibrated using the proposed algorithm

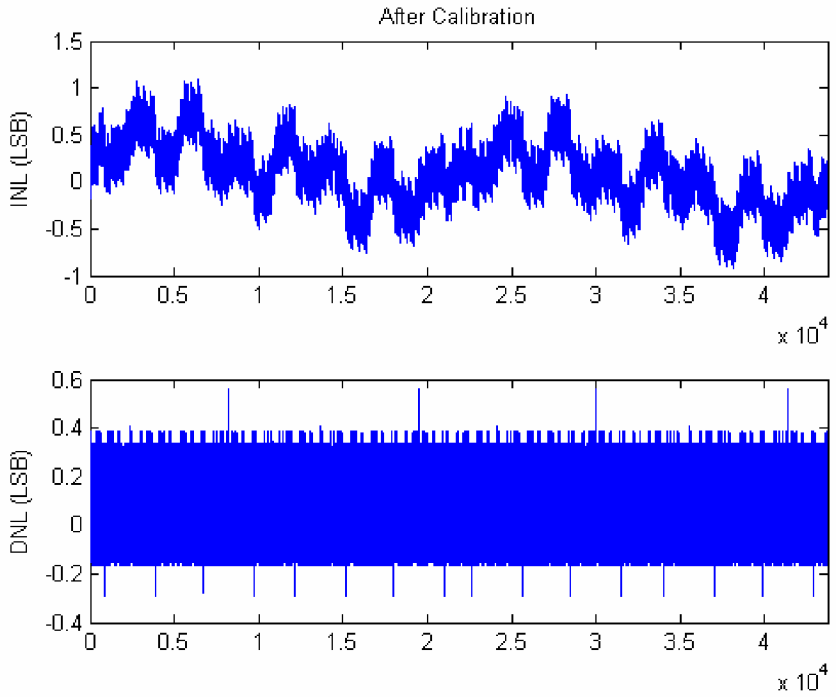

Figure 3.7 ADC's linearity after calibrated using the algorithm in [17]

3.6 Conclusion

This work presents a method for digital calibration of pipeline ADC's. With this approach, correction codes are determined using results of a special histogram code density test. In contrast to histogram-based code-density tests used in production testing of INL and DNL that require very linear excitations, this code-density test is based upon determining only the presence or absence of output codes and hence does not impose stringent requirements on the performance of the source used to generate the output codes. No disturbance of the residue path internal to the pipeline is needed for the calibration. The algorithm can significantly improve the linearity of a pipeline ADC by removing the discontinuities in the output. The digital calibration can be easily implemented on-chip with a

small amount of hardware overhead. The algorithm can be applied to pipeline or cyclic ADC architectures with 1-bit/stage sub-radix structures or to multi-bit/stage converters with over-range protection. In the latter case, some straightforward modifications to the formulation presented in this thesis are required.

CHAPTER 4 AN N^{TH}-ORDER CENTRAL-SYMMETRICAL LAYOUT TECHNIQUE FOR NONLINEAR GRADIENT CANCELLATION

This work is focused on reducing the effects of higher-order gradients on the matching performance of circuit elements. A new layout structure based upon flexible central-symmetric cell placement is proposed. Theoretical analysis shows this technique provides cancellation of up to n^{th} order gradient effects when matching two devices by using 2^n unit cells for each device. Simulation results show that the proposed technique gives better matching characteristics than other existing layout techniques in the presence of nonlinear gradients. Experimental results are presented which support the theoretical development.

4.1 Introduction

Mismatch between identically designed devices is invariably observed after fabrication and is due to the random variation in the properties of the materials used to fabricate the devices. Matching accuracy is the major factor that limits the performance of many analog and mixed signal integrated circuits. For example, matching accuracy of the sampling capacitors in the inter-stage switched-capacitor amplifiers directly affects the performance of a pipeline/cyclic analog-to-digital converter. The matching characteristic of current mirrors also plays a key role in many applications [18] [19].

Layout techniques for minimizing mismatch have become increasingly important for high performance circuit design since even a small amount of mismatch can significantly degrade the performance of a precision circuit. Over the years, great efforts have been made

in the study of mismatch and layout strategies [20]-[22]. Previous studies have shown that the causes of mismatch can be attributed to either systematic or random variations. Systematic variations are associated with inherent differences in devices associated with shape, placement, or orientation. Random variations are generally comprised of two types. One is associated with local variations where it is assumed there is no correlation between the random parts of the material properties even if the separation is quite small. A second type of random variation is associated with variations that are correlated over dimensions that exceed the dimensions of the matching-critical devices. This second type is often termed a gradient effect. The magnitude, angle, and order of the gradients are random variables at the process level but in the region of the matching-critical elements on the die, they are systematic. These gradients do vary in both magnitude and direction from one location to another on an integrated circuit. The local random variations are usually modeled with a Gaussian distribution and the impact these variations have on matching performance is determined by tradeoffs that can be made between area and matching accuracy [21]. The mismatch contribution of the gradient effects may be comparable to or even larger than that associated with the local random variations [23]. If the random mismatch effects are sufficiently reduced by increasing area, gradient induced mismatch effects become the dominant contributors to the overall mismatch. Furthermore, increasing area to reduce the effects of local random variations often makes the gradient effects more significant. Since mismatch due to gradient effects can become the dominant factor degrading matching performance, the gradient effects should be carefully characterized and methods established to minimize the effects they have on matching. Despite the widely recognized importance of matching, layout strategies dealing with the gradient effects on matching are quite limited.

Closely placing matching-critical components somehow reduces the gradient effects, but does not cancel it. It is a widely accepted belief that the common centroid layout approach, which is widely used, compensates for linear gradient [24] effects but there is little in the literature to suggest which, if any, of the common centroid techniques compensate for higher-order gradients. A circular symmetry pattern [1] has the potential to cancel nonlinear gradients, but it is not area efficient and not practical since unit cells that comprise the structure need to be placed diagonally or in some particular angle with each other, which can not be easily realized in most of today's processes. In this work, higher-order gradient effects are studied and a practical area-efficient layout strategy that compensates for nonlinear gradients up to an arbitrarily selected order n is introduced.

The rest of the chapter is organized as follows. In Section 4.2, a general mathematical model of high-order gradient effects is given. Section 4.3 describes a new layout strategy and shows how it can cancel nonlinear gradient effects. Section 4.4 provides simulation results of the proposed and existing layout strategies, respectively. Section 4.5 discusses experimental results and Section 4.6 concludes the work.

4.2 Gradient Modeling

Process parameters in semiconductor processes are often modeled by two-dimensional polynomial functions, $p(x,y)$, where (x,y) denotes lateral position relative to an arbitrarily-placed coordinate system on the die. The process parameters are distributed throughout a die. At a somewhat higher-level, the distributed process parameters in the regions occupied by devices such as resistors, capacitors, and transistors determine the parameters that are used by circuit designers in lumped models of these devices. These model

parameters include the resistance of a resistor, the capacitance of a capacitor, the threshold voltage of a MOSFET and most other parameters that are use to model these devices. Mapping between the distributed process parameters and the lumped device parameters is straightforward when the process parameters are homogeneous but can become quite complicated when the process parameters are not homogeneous. Various approximations to this mapping have been used in the literature, often without mathematical verification of the validity. No attempt will be made in this work to make a mapping between the distributed process parameters and the lumped model parameters but rather an assumption will be made that the model parameters can be modeled by a two-dimensional polynomial function evaluated at some predetermined point in the device. In what follows, devices will be comprised of parallel or series combinations of a unit cell and it will be assumed that each cell has a predetermined point (alternately reference point) that is geometrically invariant from one unit cell to the next and this point identifies the location of the unit cell on a die.

With this assumption, a two-dimension polynomial function will be used to model a device parameter P for a group of unit cells and a cell located with reference point at (x,y) will have device parameter $P(x, y)$. It will be assumed that the function $P(x,y)$ is continuous and high-order differentiable in both x and y. As such, $P(x,y)$ will be approximated by an n^{th}-order polynomial function in the variables x and y by the expression

$$P = \sum_{i=1}^{n} p_i(x, y), \tag{4.1}$$

where p_k is the k^{th}-order polynomial that comprises P and where the constant part of P is included in p_1.

A parameter that only has a linear (1^{st} order) gradient can be modeled as

$$P = p_1(x,y) = G_1(x,y) + C \tag{4.2}$$

where C is a constant that is independent of x and y. The function $G_1(x,y)$ is expressed as

$$G_1(x,y) = g_{1,0}x + g_{0,1}y \tag{4.3}$$

and is termed the 1st order gradient component of the parameter P. $g_{1,0}$ and $g_{0,1}$ are the linear gradient coefficients.

If follows from (4.1) that an nth order gradient model of the parameter P can be expressed as

$$P(x,y) = \sum_{i=1}^{n} G_i(x,y) + C\,, \tag{4.4}$$

where

$$G_i(x,y) = \sum_{j=0}^{i} g_{j,i-j}x^j y^{i-j} \tag{4.5}$$

is the i^{th} order gradient component of P. $g_{j,i-j}$ is the coefficient of the j^{th} polynomial term $x^j y^{i-j}$ in the i^{th} order component G_i.

Devices such as resistors, capacitors, and MOS transistors are generally comprised of two or more unit cells connected in either a series or a parallel configuration. It will be assumed that the corresponding parameter that characterizes the device is either the average of the parameters for each of the unit cells comprising the device or the sum of the parameters of the unit cells that comprise the device. For example, if the device is comprised as the series connection of unit cells that comprise the resistor, the resistance of the device would be the sum or the resistances of the unit cells comprising the device and if the device is a MOS transistor comprised of n units cells connected in parallel, the threshold voltage of

the resultant device would be the average of the threshold voltages of the unit cells. Since the sum and average only differ by a constant, it will be assumed for notational convenience that the parameter of interest is the sum of the parameters of the unit cells. With this assumption, consider a device composed of m unit cells located at $(x_1,y_1)\ldots(x_m,y_m)$. If up to n^{th} order gradients are taken into consideration, the device's parameter can be expressed as

$$P = \sum_{i=1}^{m} P_i(x_i, y_i) = \sum_{i=1}^{m}\sum_{j=1}^{n} p_j(x_i, y_i). \tag{4.6}$$

For two identical devices A and B, ideal matching is achieved if

$$P_A = P_B. \tag{4.7}$$

The n^{th} order gradient model of (4.4) or correspondingly the n^{th}-order gradient model of (4.6) obtained by combining m unit cells is based upon representing the gradient in an arbitrarily-placed coordinate system on the die. It will now be shown that if the order of the model is invariant to translations of the coordinate system and, as such, the order of the model will not change if the origin is moved from (0,0) in the original coordinate system to the point (x_0,y_0) where (x_0,y_0) is any other point in the original coordinate system. To show this, observe that for order m larger than 1, substituting x with $(x\text{-}x_0+x_0)$ and substituting y with $(y\text{-}y_0+y_0)$, (4.4) becomes

$$P(x, y) = \sum_{i=1}^{n}\sum_{j=0}^{i} g_{j,i-j}(x - x_0 + x_0)^j (y - y_0 + y_0)^{i-j} + C, \tag{4.8}$$

which can be rewritten as

$$P(x, y) = \sum_{j=0}^{n} g_{j,n-j}(x - x_0 + x_0)^j (y - y_0 + y_0)^{n-j} + \sum_{i=1}^{n-1}\sum_{j=o}^{i} g_{j,i-j} x^j y^{i-j} + C. \tag{4.9}$$

Define T_1 to be the 1st term on the right-hand side of (4.9). This is the term that contains the highest-order gradient effects. Expanding this term, it follows that

$$T_1 = \sum_{j=0}^{n} g_{j,n-j}\left(\left(\sum_{k=0}^{j}\binom{j}{k}x_0{}^{j-k}(x-x_0)^k\right)\times\left(\sum_{l=0}^{n-j}\binom{n-j}{l}y_0{}^{n-j-l}(y-y_0)^l\right)\right). \quad (4.10)$$

Equation (4.10) can be rewritten as

$$T_1 = \sum_{j=0}^{n} g_{j,n-j}(x-x_0)^j(y-y_0)^{n-j} + \sum_{j=0}^{n} g_{j,n-j}\sum_{k\geq 0,l\geq 0,k+l\leq n-1}\alpha_{k,l}(x-x_0)^k(y-y_0)^l, \quad (4.11)$$

where $\alpha_{k,l}$ is the coefficient of $(x\text{-}x_0)^k(y\text{-}y_0)^l$. Notice that the order of the 2nd term on the right hand side of (4.9) and the 2nd term on the right hand side of (4.11) are both no greater than (n-1). That means (4.9) can be expressed in the form

$$P(x,y) = \sum_{j=0}^{n} g_{j,n-j}(x-x_0)^j(y-y_0)^{n-j} + \sum_{i=1}^{n-1} G_i'(x,y) + C' \quad (4.12)$$

where

$$G_i'(x,y) = \sum_{j=0}^{i} g'_{j,i-j}x^j y^{i-j} \quad (4.13)$$

has the same form as $G_i(x, y)$, but with different coefficients and where C' is a constant. Equation (4.12) shows that the order of the gradient is invariant to the location of the origin of the coordinate system on the die and, as such, the order of the gradient is an inherent property of a parameter P.

4.3 Cancellation of Gradients to N^{th} Order with New Central-Symmetrical Layout Structures

A strategy for cancelling all gradients up to n^{th} order that contribute to the mismatch of two nominally identical devices will be developed in this section. This strategy will be based upon a new layout strategy that has key symmetry properties that provide this cancellation. The term "central-symmetrical" will be used to denote all layout structures that have this property. A central-symmetrical layout structure can be thought of as an extension of the concept of a common-centroid layout in the sense that central-symmetrical layouts are common-centroid layouts with sufficient additional structure to provide cancellation of all gradient effects up to n^{th} order. A description of a method for generating central-symmetrical layout structures or patterns follows:

i) The 1^{st} order form of the pattern is just any common centroid pattern. As examples, two widely-used common-centroid structures are shown in Figure 4.1. Common centroid layout patterns ensure the cancellation of linear (1^{st} order) gradient effects.

ii) An n^{th} (n>1) order central-symmetrical pattern will be defined in terms of the $(n-1)^{st}$ order pattern. To define this, we will introduce the concept of a union structure. The "union structure" for the layout of two devices is the structure obtained by neglecting the distinction between the "A" and "B" unit cells in the device. The n^{th} order pattern is composed of two $(n-1)^{st}$ order patterns whose union structures are symmetrical to a center C_n. The parity of n will now be considered in creating the n^{th}-order central-symmetric structure from the symmetrical union structures.

a) If n is odd, the unit cells of each device are central-symmetrical around C_n. That means for each unit cell of device A with reference point P, there is another unit cell of device A with reference point P' and the mid-point of segment PP' is exactly the symmetrical center C_n.

b) If n is even, the unit cells of the two devices in one of the $(n-1)^{st}$ order patterns should be interchanged so that the position of device A's unit cells are central-symmetrical to device B's unit cells around C_n. That means for each unit cell of device A with reference point P, there is an unit cell of device B with reference point P' and the mid-point of segment PP' is exactly the symmetrical center C_n. Figure 4.2 and Figure 4.3 show some high order ($n \geq 2$) central-symmetrical layout patterns.

It will now be shown that nonlinear gradient effects up to order n are cancelled with n^{th} order central-symmetrical layout structures.

Suppose device A and device B are each comprised of *m* unit cells.

i) If n=1, the parameter only has linear gradient effect. According to (4.6), the parameter of device A is

$$P_A = \sum_{i=1}^{m} P_{Ai}\left(x_{Ai}, y_{Ai}\right) = \sum_{i=1}^{m} \left(g_{1,0} x_{Ai} + g_{0,1} y_{Ai} + C\right) \tag{4.14}$$

Similarly, the parameter of device B is

$$P_B = \sum_{i=1}^{m} P_{Bi}\left(x_{Bi}, y_{Bi}\right) = \sum_{i=1}^{m} \left(g_{1,0} x_{Bi} + g_{0,1} y_{Bi} + C\right) \tag{4.15}$$

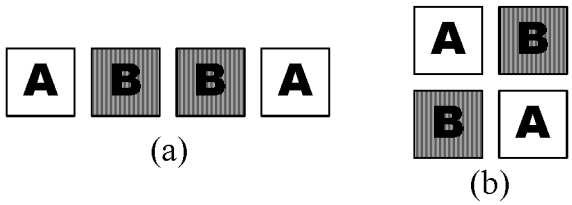

Figure 4.1 Examples of 1st order central-symmetrical pattern

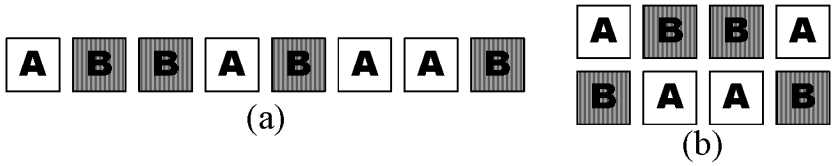

Figure 4.2 Examples of 2nd order central-symmetrical pattern

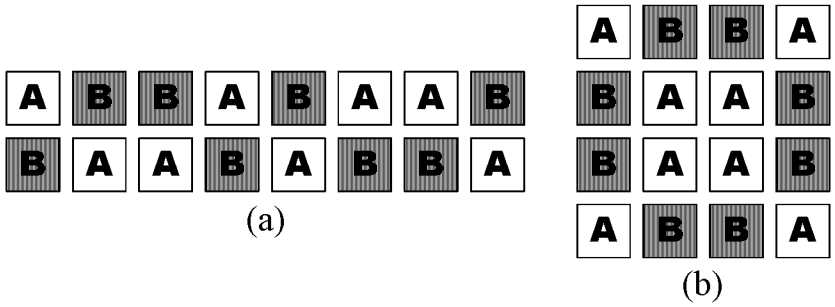

Figure 4.3 Examples of 3rd order central-symmetrical pattern

The centroid of a device composed of m unit cells with reference points located at (x_i, y_i), $i=1,2,\ldots,m$ is defined to be (x_c, y_c) where

$$x_c = \frac{1}{m}\sum_{i=1}^{m} x_i \tag{4.16}$$

$$y_c = \frac{1}{m}\sum_{i=1}^{m} y_i \tag{4.17}$$

From (4.14) ~ (4.176), it is not difficult to show that (4.7) holds for arbitrary gradient magnitudes and arbitrary gradient directions if and only if $x_{cA}=x_{cB}$ and $y_{cA}=y_{cB}$. This is why a common centroid layout structure provides for cancellation of linear gradient effects.

ii) If n>1, since the higher-order patterns are constructed by duplicating lower-order patterns, the number of unit cells of each device, *m*, must be an even number. Now consider two cases depending upon the parity of *n*:

a) If n is odd

Consider device A, according to the layout pattern, for a unit cell A_i with reference point at (x_{Ai}, y_{Ai}), there must be another unit cell A_{m-i} with reference point at (x_{Am-i},y_{Am-i}) such that $x_{Ai}-x_{Cn}=x_{Cn}-x_{Am-i}$ and $y_{Ai}-y_{Cn}=y_{Cn}-y_{Am-i}$. Thus for any $0 \le j \le n$,

$$(x_{Ai}-x_{Cn})^j (y_{Ai}-y_{Cn})^{n-j} = -(x_{Am-i}-x_{Cn})^j (y_{Am-i}-y_{Cn})^{n-j} \tag{4.18}$$

Locating the coordinate system by choosing x_0 and y_0 in (4.11) to be x_{Cn} and y_{Cn} and then it follows from (4.18), (4.12) and (4.6) that

$$P_A = \sum_{i=1}^{m}\sum_{j=1}^{n-1}\left(G'_j(x_{Ai}, y_{Ai})+C'\right) \tag{4.19}$$

Since unit cells of device B have the same central symmetry property,

$$P_B = \sum_{i=1}^{m}\sum_{j=1}^{n-1}\left(G'_j(x_{Bi}, y_{Bi})+C'\right) \tag{4.20}$$

From (4.19) and (4.20), the difference between the parameter of device A and the parameter of device B is given by

$$P_A - P_B = \sum_{i=1}^{m}\sum_{j=1}^{n-1}\left(G'_j(x_{Ai}, y_{Ai})-G'_j(x_{Bi}, y_{Bi})\right) \tag{4.21}$$

which means the mismatch due to the n^{th} order gradient effect has been cancelled for n odd.

b) If n is even

According to the layout pattern, for a unit cell in device A with reference point at (x_{Ai}, y_{Ai}), there is a corresponding unit in device B with reference point at (x_{Bi}, y_{Bi}) such that x_{Ai}-x_{Cn}=x_{Cn}-x_{Bi} and y_{Ai}-y_{Cn}=y_{Cn}-y_{Bi}. Then for any $0 \le j \le n$

$$(x_{Ai} - x_{Cn})^j (y_{Ai} - y_{Cn})^{n-j} = (x_{Bi} - x_{Cn})^j (y_{Bi} - y_{Cn})^{n-j} \tag{4.22}$$

Locating the coordinate system by choosing x_0 and y_0 in (4.12) to be x_{Cn} and y_{Cn} and substituting (4.12) to (4.6), the parameters of device A and device B are given by

$$P_A = \sum_{i=1}^{m} \left(\sum_{j=0}^{n} g_{j,n-j} (x_{Ai} - x_{Cn})^j (y_{Ai} - y_{Cn})^{n-j} + \sum_{j=1}^{n-1} G'_j (x_{Ai}, y_{Ai}) + C' \right) \tag{4.23}$$

and

$$P_B = \sum_{i=1}^{m} \left(\sum_{j=0}^{n} g_{j,n-j} (x_{Bi} - x_{Cn})^j (y_{Bi} - y_{Cn})^{n-j} + \sum_{j=1}^{n-1} G'_j (x_{Ai}, y_{Ai}) + C' \right) \tag{4.24}$$

If follows from (4.22) -(4.24) that (4.21) is still satisfied. Thus, the mismatch due to the n^{th} order gradient effect is cancelled for n even.

Since the n^{th} order layout pattern is built from the $(n-1)^{st}$ order layout pattern, which will cancel the $(n-1)^{st}$ order gradient effect, the n^{th} order pattern should preserve this property and also be able to cancel the $(n-1)^{st}$ order gradient. Following this argument, it follows that 1^{st} through n^{th} order gradient effects are cancelled with an n^{th} order central-symmetrical layout structure.

These observations can thus be summarized in the following two theorems. The first is a formalization of properties of common-centroid layouts that are well known. The latter is a new contribution coming from this work.

Theorem 1

If only linear gradient effects are present in the region where two devices are placed, then the mismatch of a parameter *f* between two nominally identical elements will vanish if a common-centroid layout is used.

Theorem 2

If only gradients up to order m are present in the region where two devices are placed, then the mismatch of a parameter *f* between two nominally identical elements will vanish if the layout is central-symmetrical of order n.

Clarifications need to be made regarding the difference between this approach and the traditional approach for handling mismatch. Traditional approach of modeling mismatch usually makes the following assumptions: First, there is some physical parameter of the process that has some gradient and the gradient is mainly 1st order (linear) with negligible higher order terms. Second, the equivalent physical parameter for a device at a particular location and of a particular shape is a simple function of the device area or location (averaged integration of the local parameter value over the device area is usually taken without justification). The previous two assumptions usually results in an equivalent physical parameter that is the physical parameter value of a reference point of the device. The third assumption is that there exists simple relationship between the physical parameter and the electrical parameter whose mismatch we really care so that the gradient of the electrical parameter is mainly determined by the gradient of the physical parameter and they have the

same function form. Under these assumptions, common-centroid layout was claimed to be able to cancel the effect of linear gradient in physical parameter. However, some of these assumptions are made from conjecture without a good reason. Therefore a conclusion based on a bunch on questionable assumptions is doubtable. The first assumption is usually valid for a well controlled process. However, a common exception is that the thermal gradient around a power device is usually of high order. The second assumption is not obvious and is probably not valid in many cases. Taking integration over the whole area is definitely one way of taking count of each point's contribution, but not the only way and the reason why a function form is taken for the modeling purpose needs to be justified by theoretical analysis. The third assumption is not solid either. Even if the gradient in the physical parameter is the major source of the gradient in the electrical parameter, that does not imply any simple relationship between the functional form of the two gradients. A physical parameter that has linear gradient does not necessarily result in a linear gradient in the electrical parameter we want to match. The actual functional form of the gradient of the electrical parameter might be much more involved than that of the physical parameter due to the complicated mapping between them. Even if the two gradients seem to have strong correlation in some experiments, the modeling used in the second assumption need to be carefully studied to explain the result. The claim that common-centroid layout can cancel the mismatch caused by linear gradient in physical parameters is actually not valid in many cases. Its capability of canceling gradient effect is only limited to the linear gradient exist in the electrical parameter itself.

The proposed approach does not try to match two devices by canceling the gradient effect in the physical parameters since the mapping between the physical parameter and electrical parameter changes is usually complicated and changes with different cases. The

proper modeling of this mapping is another topic worth studying but is out of the focus of this work. This approach only looks at the gradient effect exists in the electrical parameter itself while the relationship between the physical parameter's gradient and electrical parameter's gradient is untouched and assumed unknown. The reason for doing this is that it is the electrical parameter that we really want to match. This also generalizes the matching problem while avoiding going into details of different physical parameter dependence behind each different electrical parameters. Hence no effort was taken to model any such physical parameter dependence and no sloppy assumption was made on this dependence either since it is unnecessary. Although the mapping from the physical parameter to the electrical parameter is unknown, the electrical parameter will always show some gradient for devices spread out over an area and the order of this gradient is unknown either. However, the proposed layout pattern is still useful for improving the matching accuracy. Suppose a linear gradient in the physical parameter results in a 5th order gradient in the electrical parameter itself. Then we know that the 5th order pattern can ensure perfect matching. Even if 5th order pattern can not be used in layout, we know that 4th order pattern will give a better matching result than the 3rd order one and the 3rd order one will be better than the 2nd order one. Obviously all these higher order patterns are better than common-centroid pattern. When doing this, how well the physical parameter is matched is not considered and is not of concern, since the increase in matching accuracy with the order number is inherently not affected by that.

4.4 Comparison of Different Layout Patterns and Simulation Results

To evaluate the performance of the proposed layout technique, we did simulations of several existing layout structures and the proposed center-symmetric approach under different gradient conditions. The layouts we considered included 1^{st} order (common centroid) through 5^{th} order central-symmetrical structures. The structures of Figure 4.4 (a) - (e) are center-symmetric structures of order 1 through 5 respectively. A 2^{nd} order circular symmetry pattern [1] is shown in Figure 4.4(f)) and a hexagonal tessellation [1] structure is shown in Figure 4.4(g). In an attempt to make a fair comparison, the same total device area was allocated for each layout structure. The center of all the test structures were placed at (0,0) so that the gradient effects to all the test structures would be similar. All the coefficients of the gradients were randomly generated and these values should not affect the validity of the simulation results since these coefficients are unknown in real case. The simulation results from one typical run are summarized in Table 4.1.

Simulation results show that for n=1,…,5, the n^{th} order gradient effects are cancelled for the central-symmetrical pattern of order n. This is consistent with the previous analysis. When using the hexagonal tessellation [1], only 2^{nd} order gradient effects are cancelled. Simulation results also show that all gradient effects up to 3^{rd} order are cancelled with the circular symmetry pattern. This is because in this pattern the placement of the unit cells of a device is central-symmetrical around the center of the circle. Then according to the analysis in Section 4.2 and 4.3, it should also cancel the 3^{rd} order gradient. Compared with existing

layout techniques, the proposed central-symmetrical layout is more area efficient and flexible in cell placement. And it is easy to be extended to cancel any high order gradient effects.

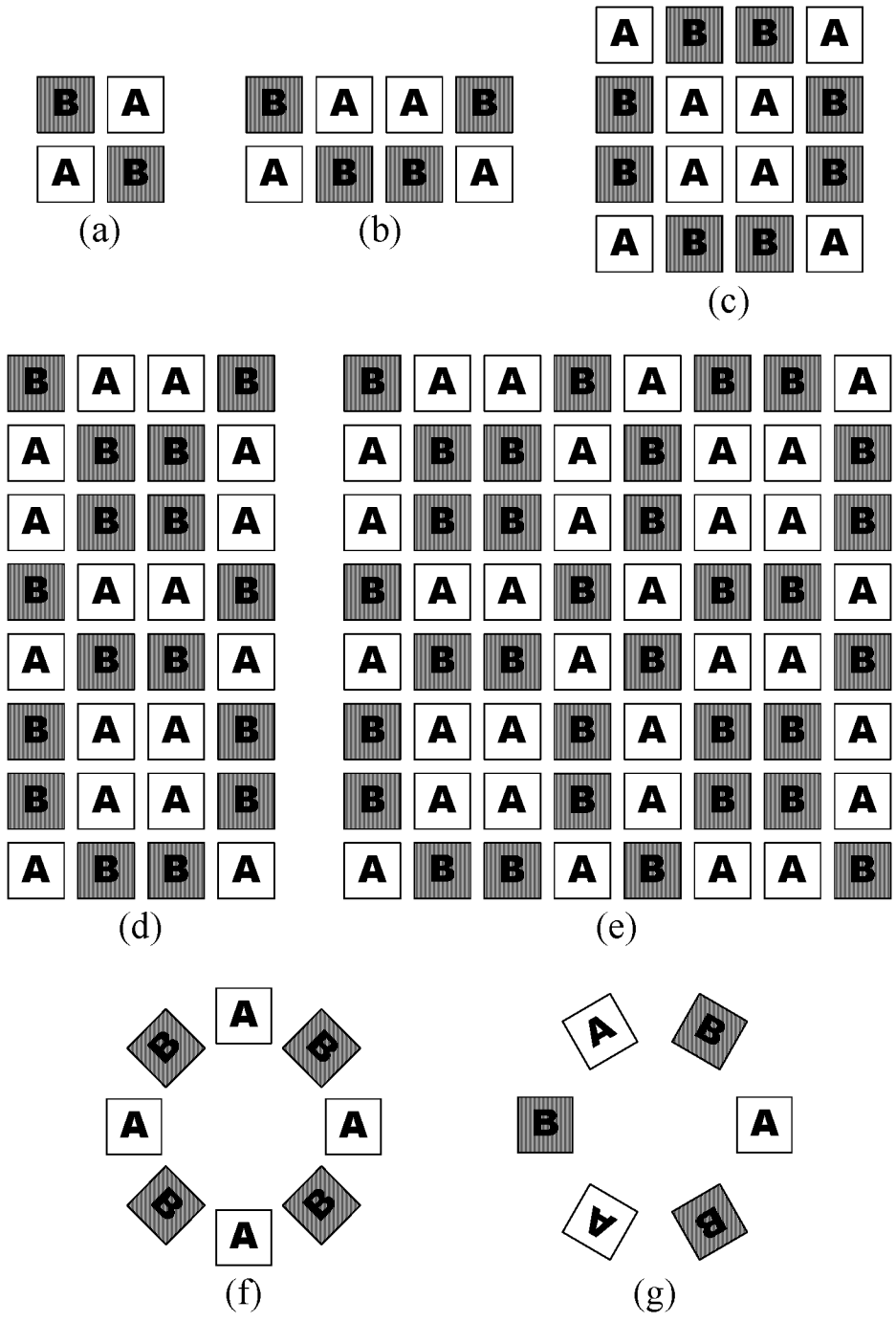

Figure 4.4 Six layout patterns used in simulation

Table 4.1 Simulation results of different layout patterns

Mismatch (%)	Highest Order of Gradient Effect				
	1^{st}	2^{nd}	3^{rd}	4^{th}	5^{th}
Figure 4.4 (a)	0	2.77	5.22	7.43	10.39
Figure 4.4 (b)	0	0	0.24	0.87	1.70
Figure4. 4 (c)	0	0	0	0.01	0.068
Figure 4.4 (d)	0	0	0	0	0.0023
Figure 4.4 (e)	0	0	0	0	0
Figure 4.4 (f)	0	0	0	0.026	0.18
Figure4.4 (g)	0	0	0.26	0.50	2.24

4.5 Experimental Results[25]

Several poly resistors were laid out in the TSMC 0.13 process using the proposed central-symmetrical layout. A test structure in a process run supported by Silicon Labs Inc was used to validate the concepts. For comparison, two pairs of resistors were laid out, one using the 2nd order pattern and the other using the 3rd order pattern, while the total area for the two pairs remained the same. The layout of the two resistor pairs is illustrated in Figure 4.5. For the 2nd order pattern shown in Figure 4.5, each resistor was formed by paralleling 4 unit cells and each unit cell took 1/8 of the total area. For the 3rd order pattern shown in Figure 4.5, each resistor was formed by parallel-series connection of 8 unit cells and each unit cell took 1/16 of the total area. More than 100 chips were measured and the systematic

mismatch data was extracted based on the model provided by the foundry. The measurement results showed that the resistor pair laid out using the 3rd order central-symmetric structure provided better matching that the structure with a 2nd order central-symmetric pattern. Due to intellectual property restrictions, details of the measured results can not be presented beyond the statement that experimental results are consistent with those predicted from the theoretical analysis introduced in this thesis.

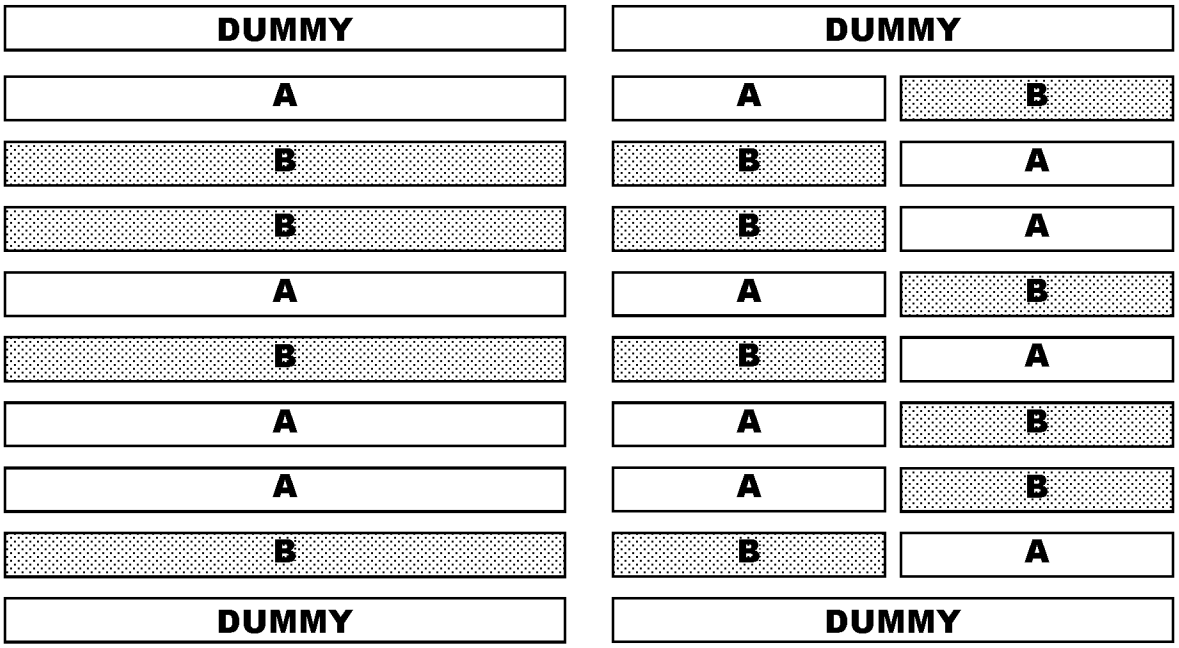

Figure 4.5 Resistor placement in layout

4.6 Conclusion

The effects of higher-order gradients in model parameters were analytically characterized. Based on this analysis, a practical and area efficient nth order central-symmetrical layout structure was introduced. In the implementation discussed in this thesis,

the n^{th} order structure requires 2^n unit cells for each device. It was shown that all gradient effects up to those of order n are cancelled with the central-symmetric layout structures. The proposed center-symmetric layouts are practical and provide excellent matching between two identically designed devices provided the order of the central-symmetric layout equals or exceeds the order of the largest gradient in the layout.

CONCLUSIONS

Characteristics of bandgap references are explored and analyzed. Instead of the commonly used V_{BE} involved approximate expression of the reference voltage output, an explicit close-form expression which is only dependent on process and model parameters are derived based on accurate modeling of bandgap references. Within the context of this explicit relationship, temperature stability properties of references are explored. This work provides improved insight into performance potential and limitations of bandgap architectures and is useful for the design of high-performance bandgap references.

A self-calibration algorithm that corrects the linearity errors of pipeline ADCs with a sub-radix architecture was developed. The algorithm uses the histogram result of simple code density test, calculates correction codes for transitions in pipeline stages, and digitally calibrates ADC's output codes. Simulation results show that the calibration algorithm can dramatically improve the linearity performance of ADCs. Since the calibration algorithm requires only a small number of memory locations and simple logic during normal operation, this method offers potential for providing a self-calibration solution for high-speed high-precision pipeline ADCs.

The effects of higher-order gradients on the matching of two nominally identical devices were discussed. A new layout methodology that provides for cancellation of all gradient effects up to a predetermined order n for two nominally identical circuit elements was introduced. As feature size continue to shrink and performance requirements continue to increase, the design and layout of high precision nominally-matched components is becoming increasingly difficult. By making use of digital calibration and the geometric

characteristic of central-symmetrical layout methods, we believe the proposed digital calibration algorithm for ADCs and the central-symmetrical layout pattern provide some insights about how to design and layout high precision circuits.

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